

Hadley15" Schematics Document

Haswell ULT

2013-06-21
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: Optimus solution installed.
eDP: Support eDP Panel installed.
LVDS: Support LVDS Panel installed.

<Core Design>



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Title

Cover Page

Size
A3

Document Number

Hadley 15"

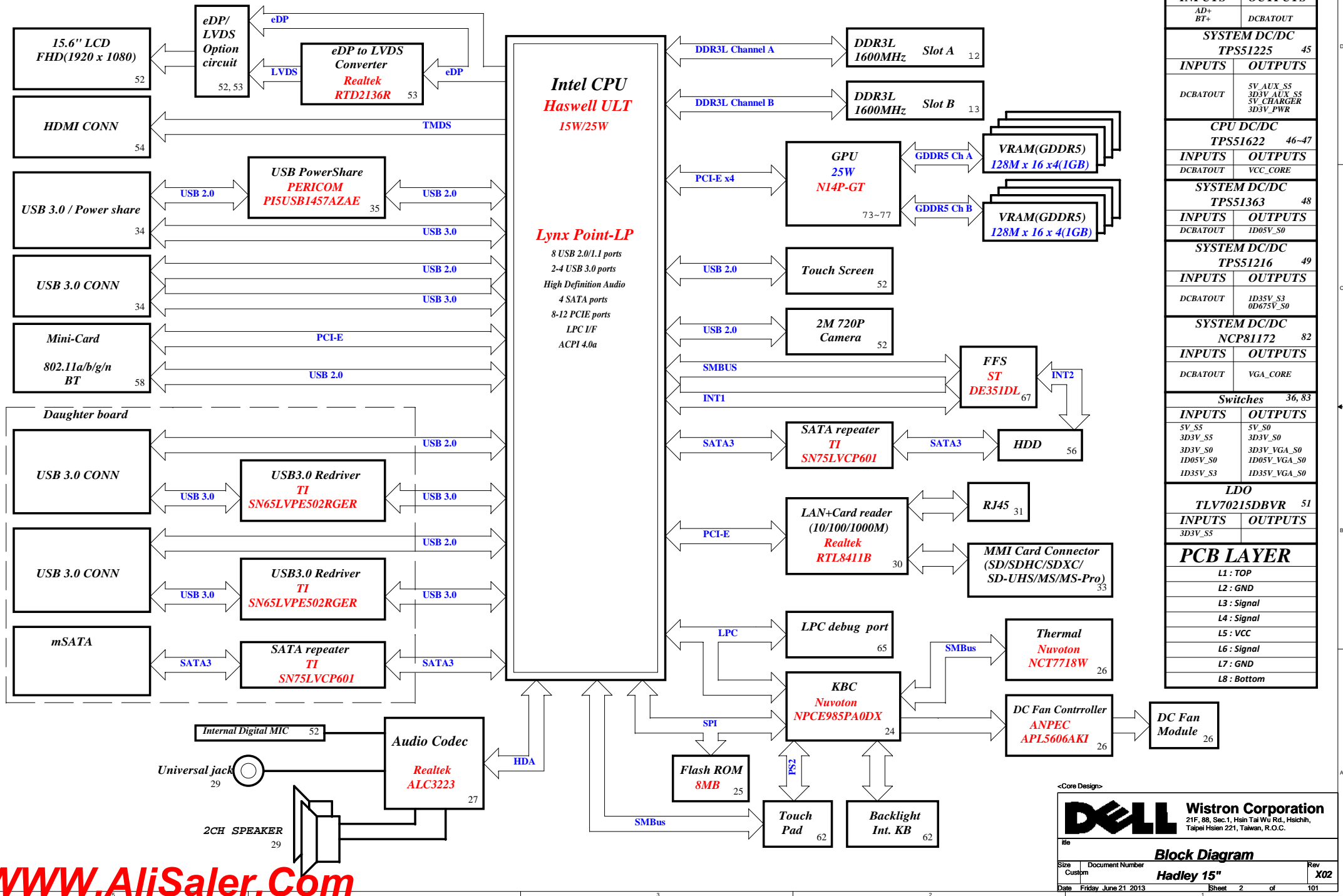
Rev
X02

Date **Friday, June 21, 2013**

Sheet **1** of **101**


Hadly15 Block Diagram

Project code : 91.47L01.001
PCB P/N : 12311-1
Revision : A00



(Blanking)

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Size

A3

Document Number

Hadley 15"

Date

Friday, June 21, 2013

Rev

X02

Sheet

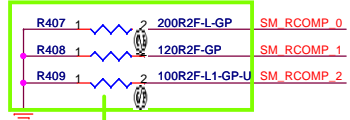
3

 of

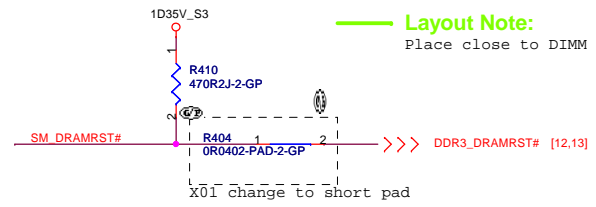
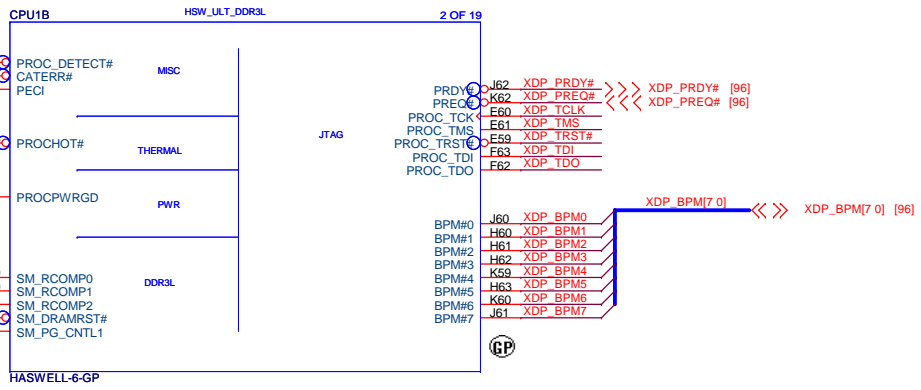
101

SSID = CPU

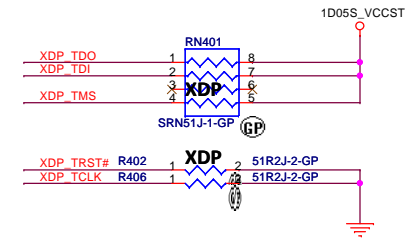
[24,42,44,46] H_PROCHOT# <<<>>>
Layout Note:
Impedance control:50 ohm



Layout Note:
Design Guideline:
SM_RCOMP keep routing length less than 500 mils.



Layout Note:
Place close to DIMM



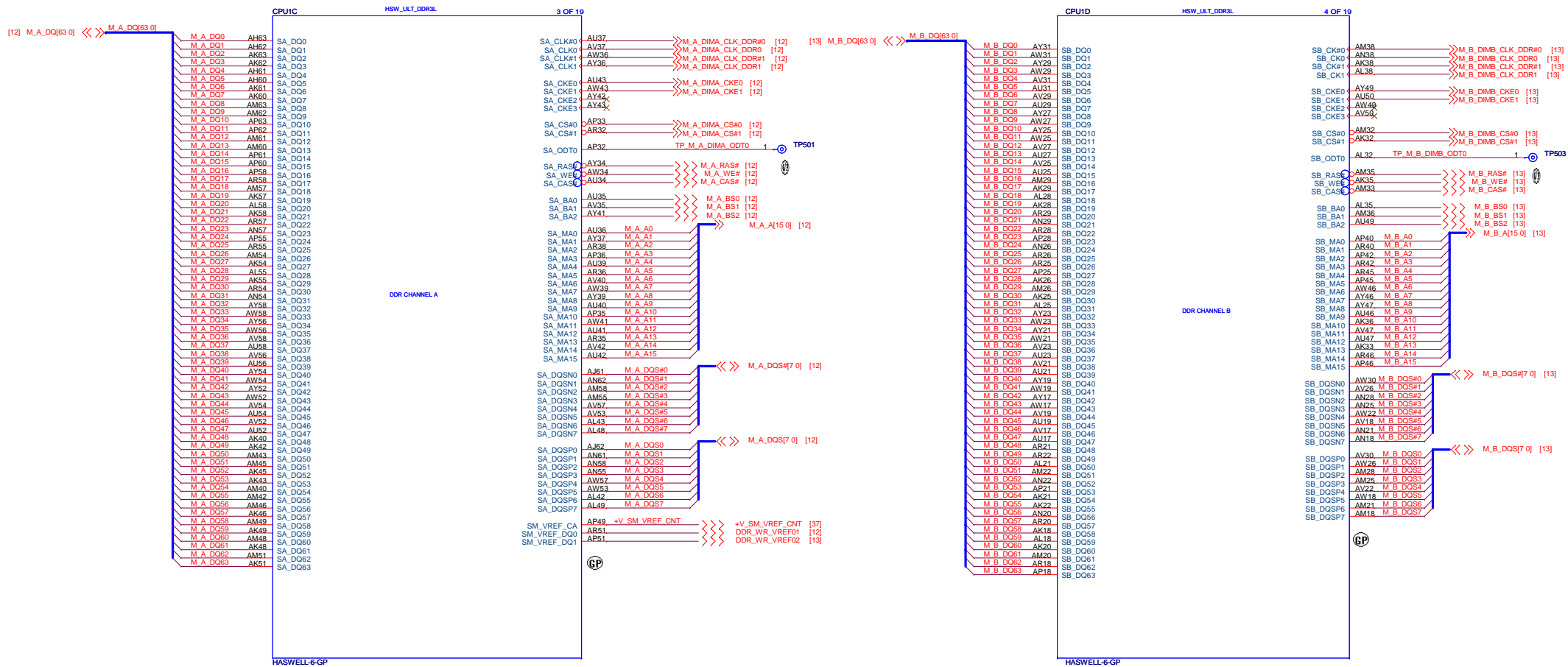
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CPU (THERMAL/CLOCK)

Size A3	Document Number	Rev X02
Date Friday, June 21, 2013	Hadley 15"	Sheet 4 of 101

SSID = CPU



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Title

CPU (DDR)

Size	Document Number
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Hadley 15"

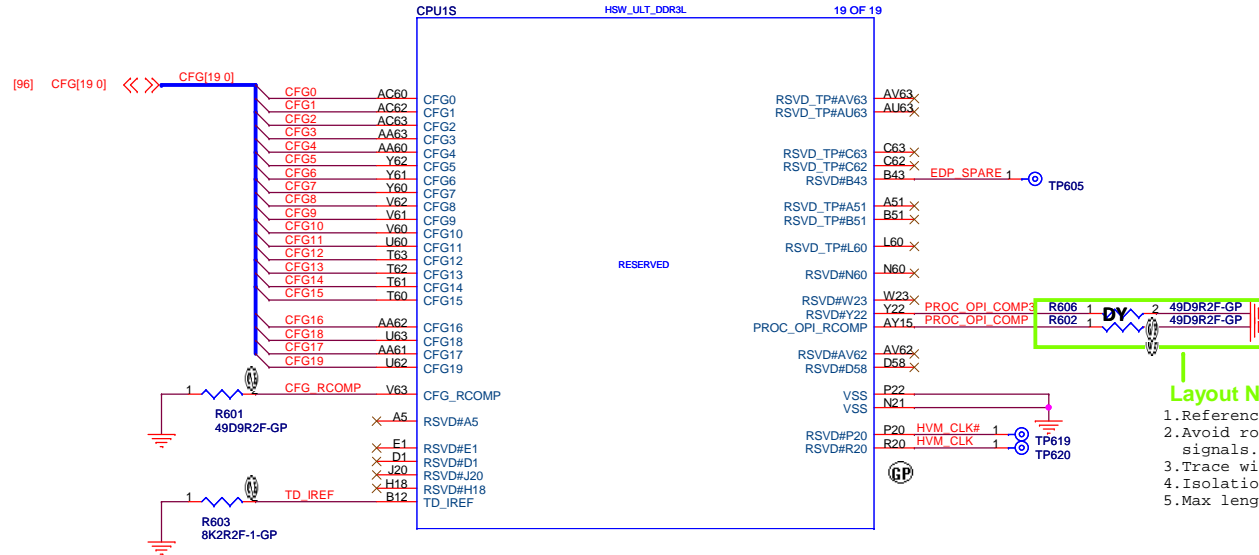
Rev

Date Friday June 21 2013

Sheet 5 of

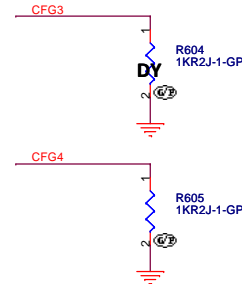
101

SSID = CPU



Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)

CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

DISPLAY_PORT_PRESENCE_STRAP

CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

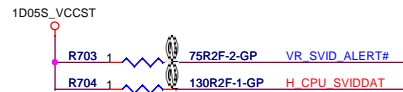
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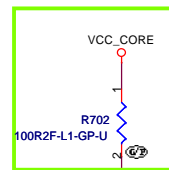
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CPU (RESERVED)				
Size A3	Document Number Hadley 15"			Rev X02
Date	Friday, June 21, 2013	Sheet	6 of	101

SSID = CPU

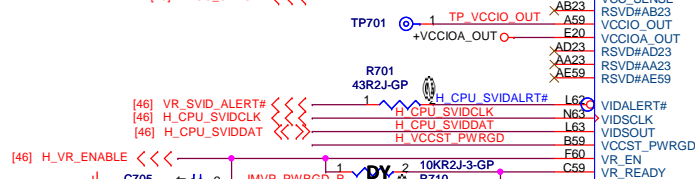


Layout Note:

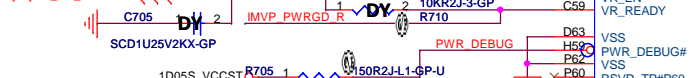
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Lwnngth match<25mil



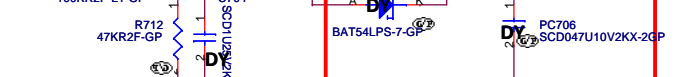
[46] VCC_SENSE <<<



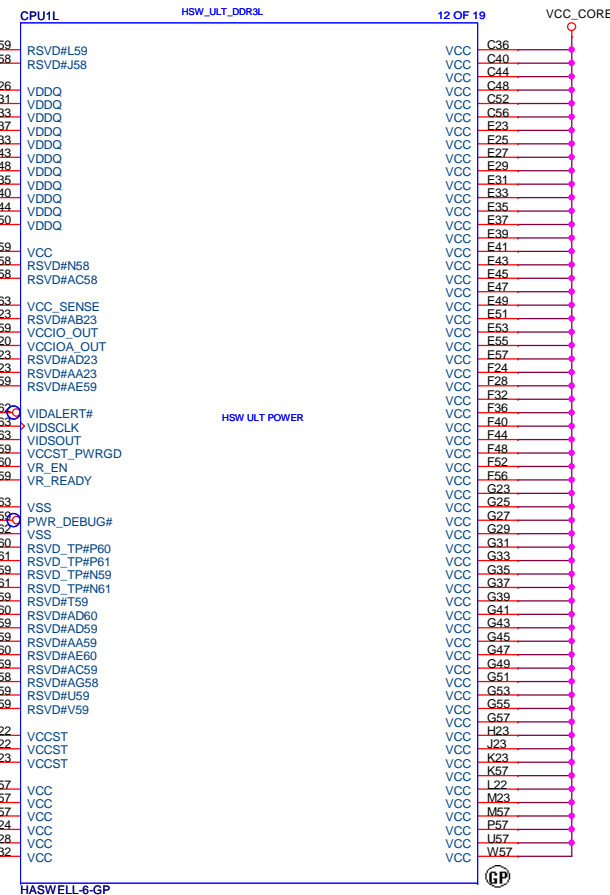
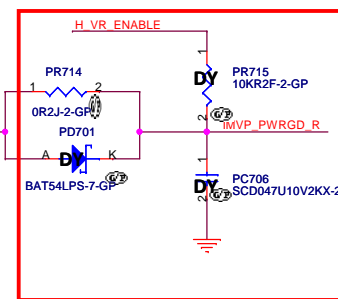
[46] H_VR_ENABLE <<<



[36,48] 1D05S_VTT_PWRGD >>>



A00 0619



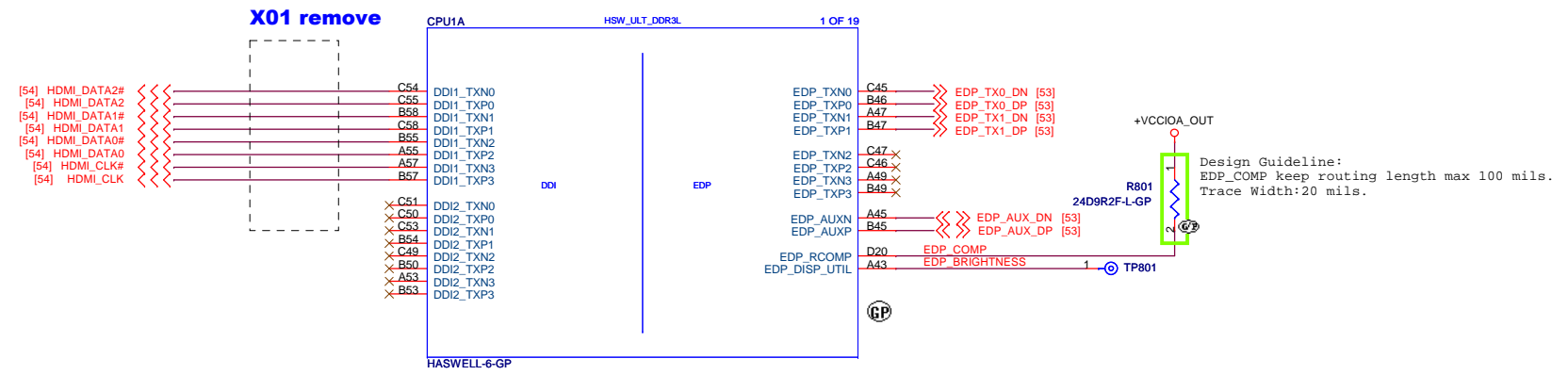
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Title		
CPU (VCC CORE)		
Size A3	Document Number	Rev X02
Date Friday, June 21, 2013	Sheet 7	of 101

SSID = CPU

HDMI



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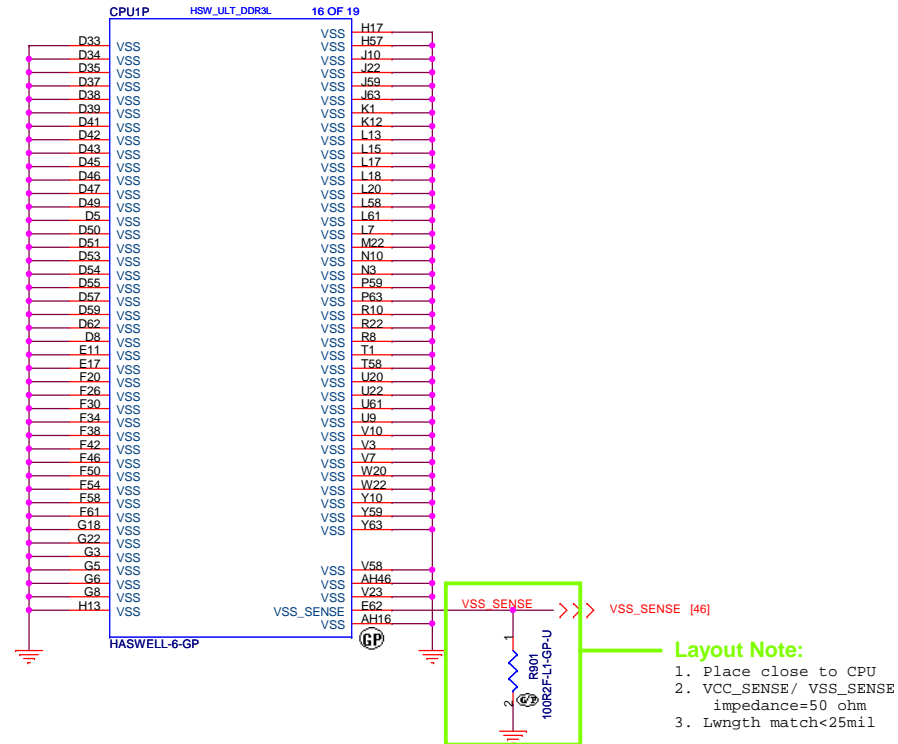
CPU (DDI/EDP)

Hadley 15"

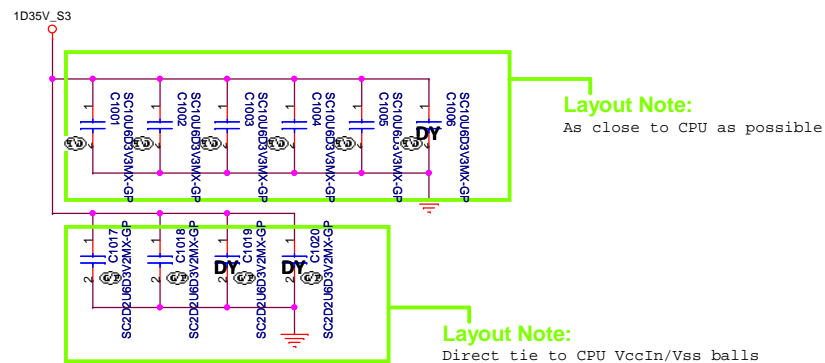
Size A3 Document Number Rev X02

Date Friday, June 21, 2013 Sheet 8 of 101

SSID = CPU



SSID = CPU



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Title

CPU(Power CAP1)

Size
A3

Document Number

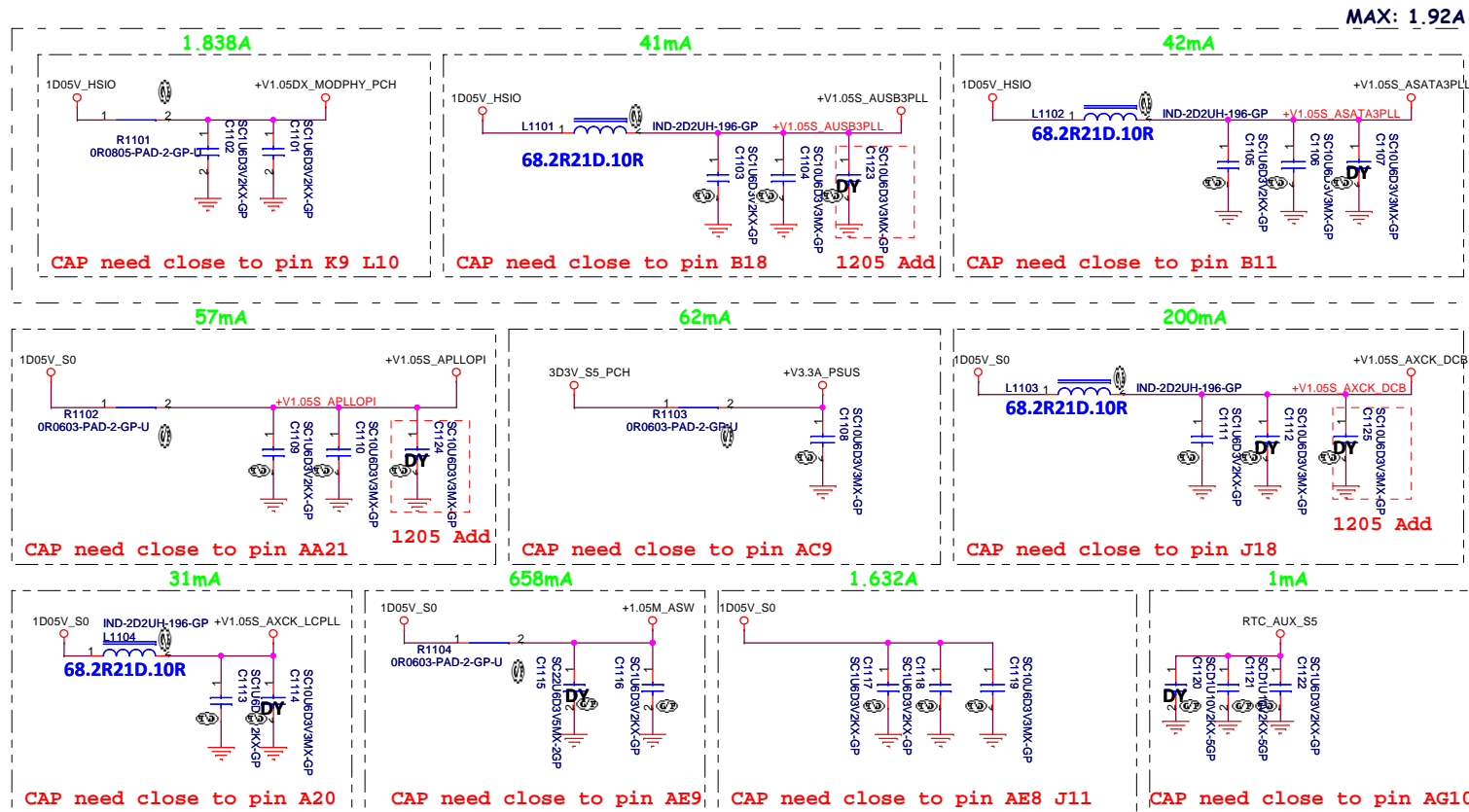
Hadley 15"

Rev
X02

Date Friday, June 21, 2013

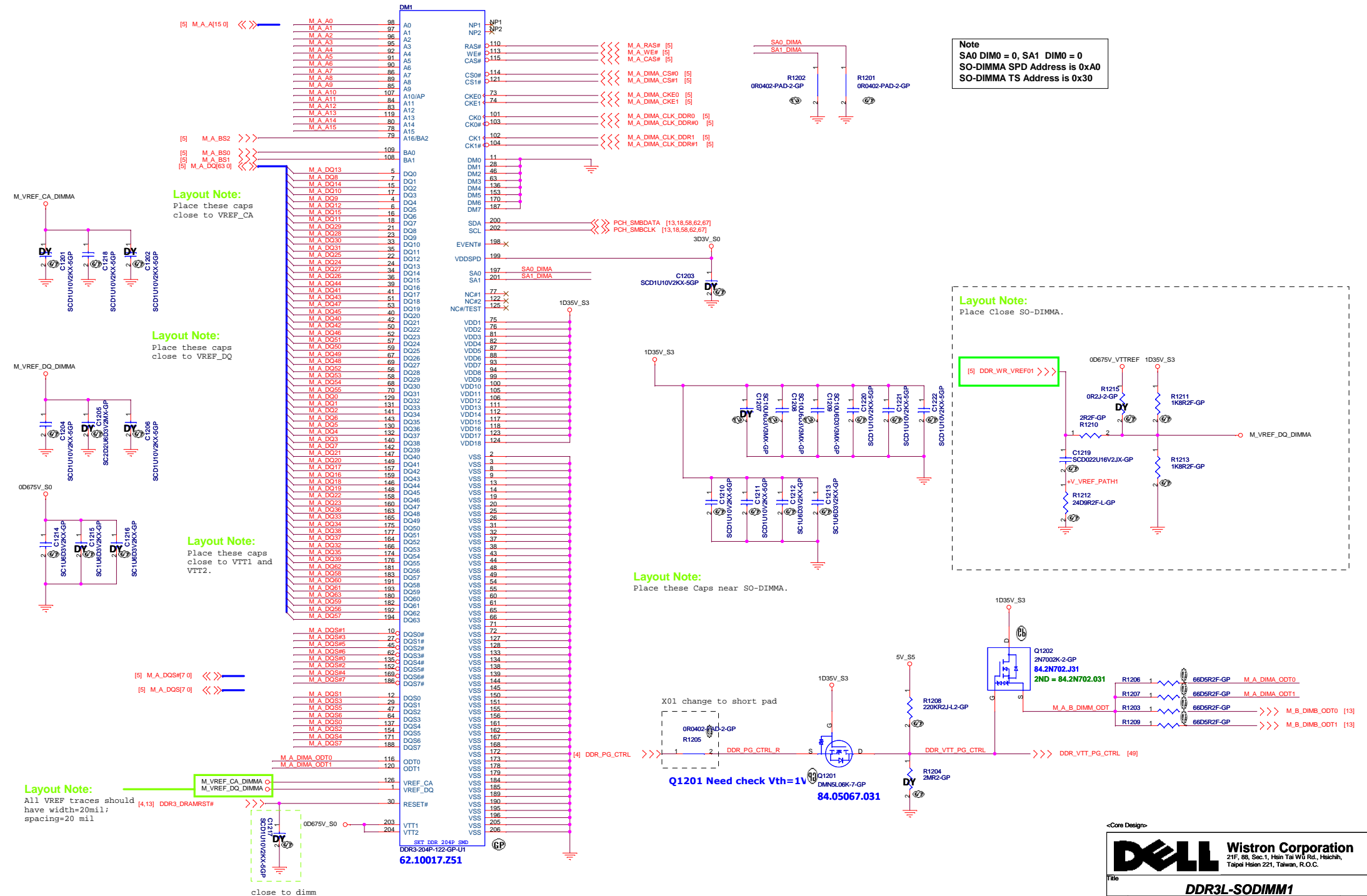
Sheet 10 of 101

SSID = CPU

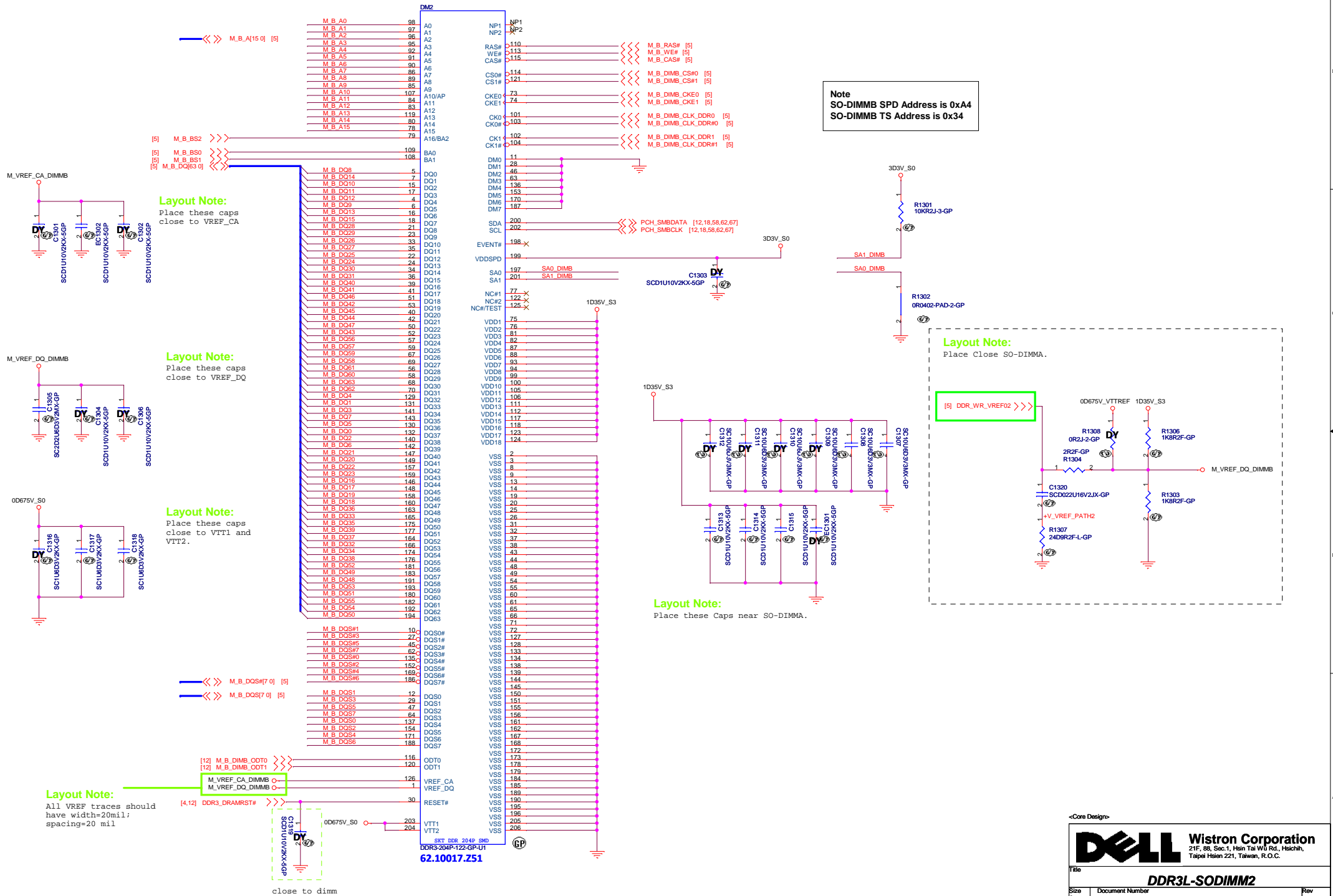


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SSID = MEMORY




SSID = MEMORY



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<Core Design>



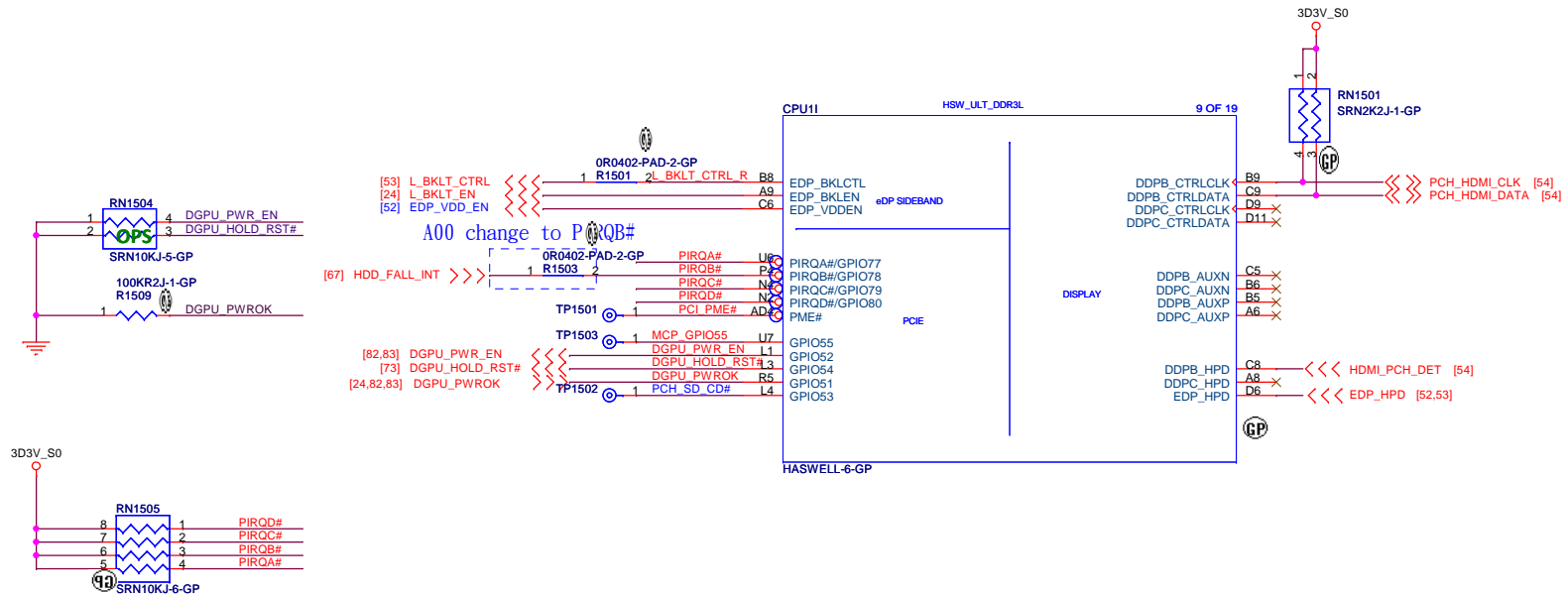
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Title

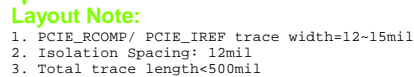
M1&M3

Size A3	Document Number Hadley 15"	Rev X02
Date Friday, June 21, 2013	Sheet 14	of 101

SSID = CPU

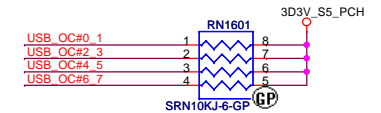


Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN+ Card reader	
5(4lane)	GPU	
6(4lane)	N/A	SATA0~3



Pair	Device
0	USB3.0 Port2
1	USB3.0 port1 (with Power Share)
2	USB3.0 Port3
3	USB3.0 Port4
4	CAMERA
5	WLAN
6	Touch Panel
7	N/A

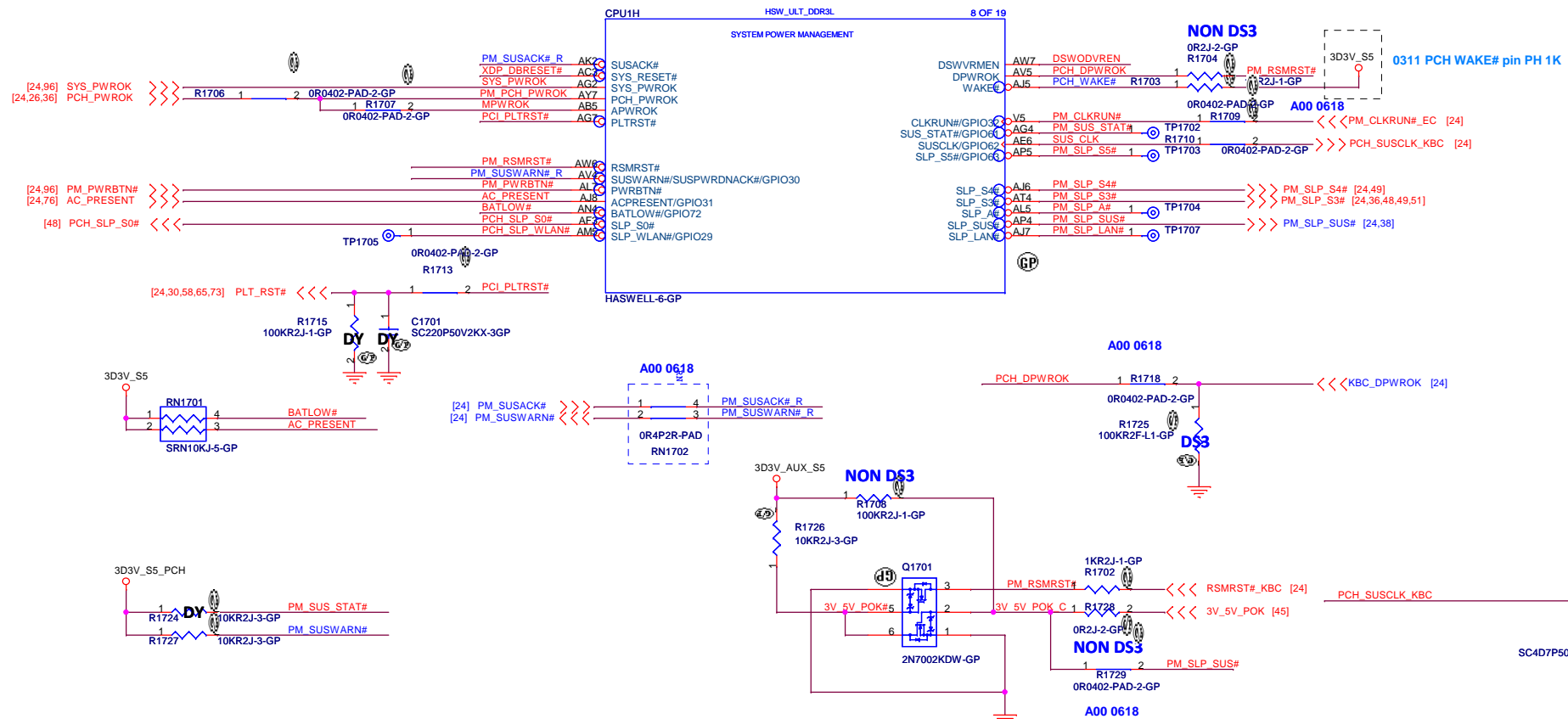
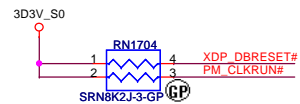
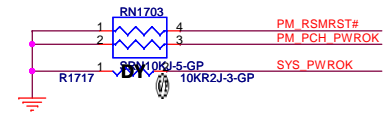
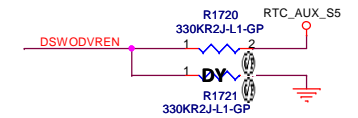
1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil



SSID = CPU

PCH strap pin:

On Die DSW VR Enable	
DSWODVREN	Low = Disable * High = Enable (default)



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CPU (PM)

Size
A

Document Number

Hadley 15"

Rev
X02

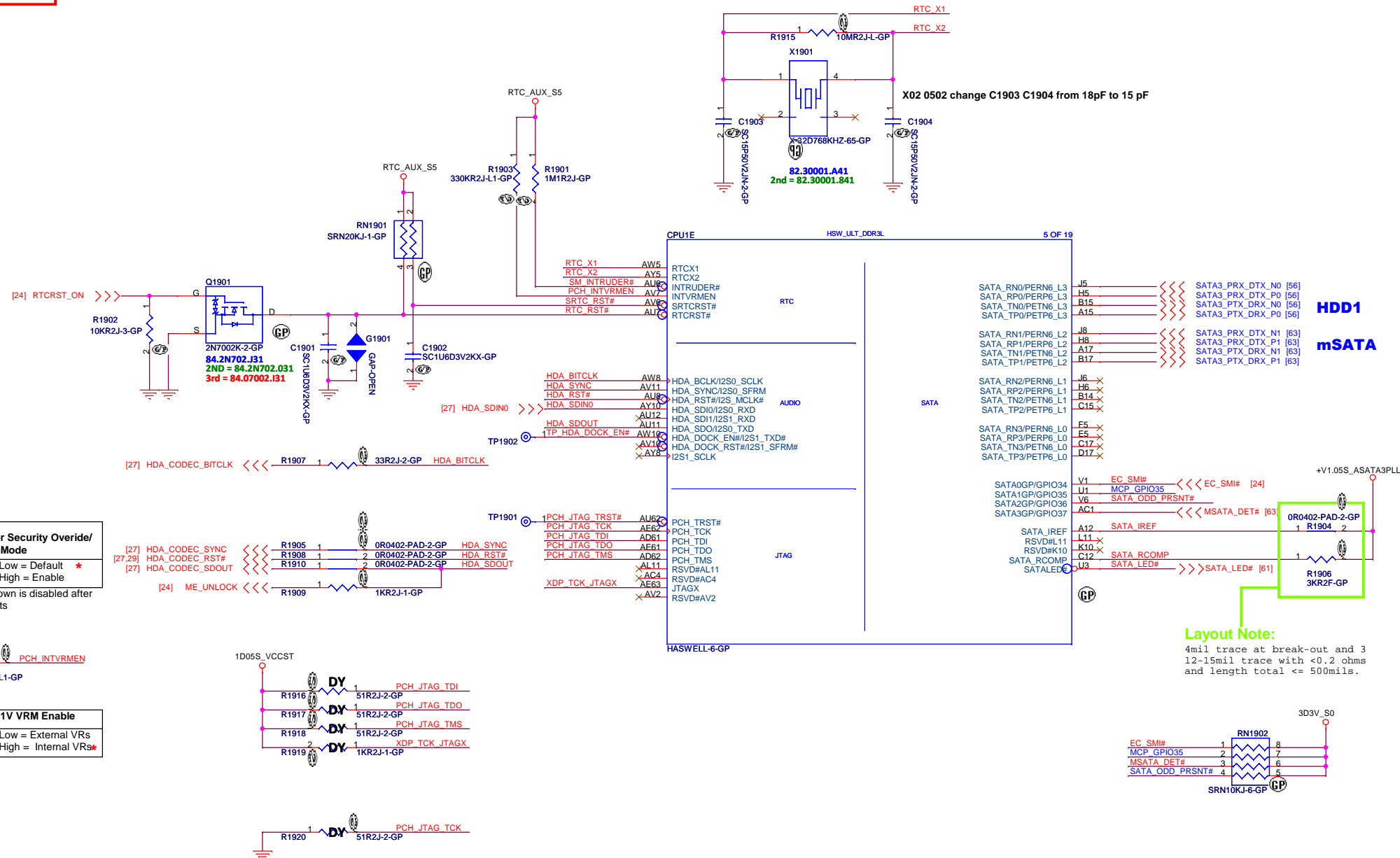
Date Friday, June 21, 2013

Sheet 17 of 101

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SSID = CPU



Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

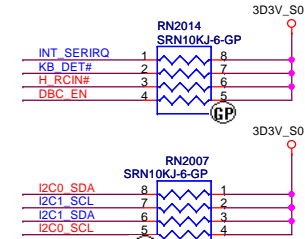
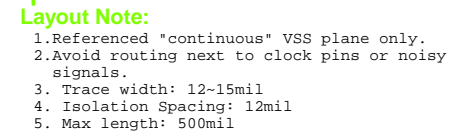
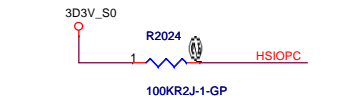
Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

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Title		CPU (RTC/SATA/HDA/JTAG)		Rev
Size	Document Number	Hadley 15"		X02
Date	Friday, June 21, 2013	Sheet	19 of	101

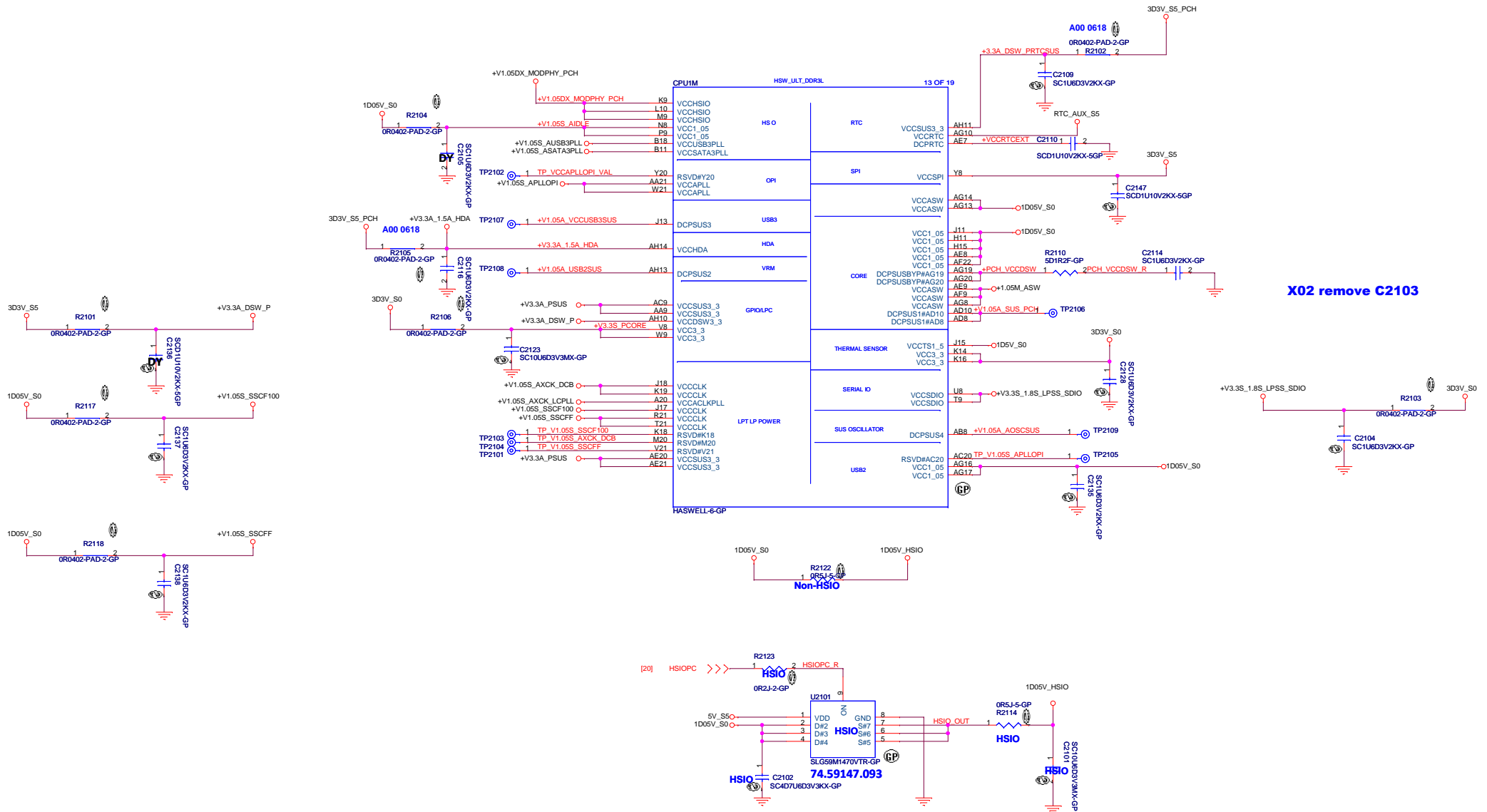
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BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
PX(AMD)	0	0
DIS	0	1
UMA	1	0
Optimus(NV)	1	1



SSID = CPU



X02 remove C2103

1 QR5J-5-GP
Non-HSIO

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Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	
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CPU (POWER2)

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Size	Document Number
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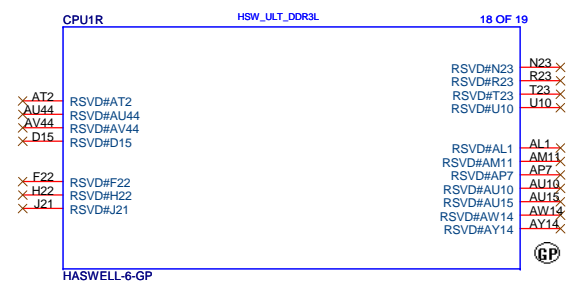
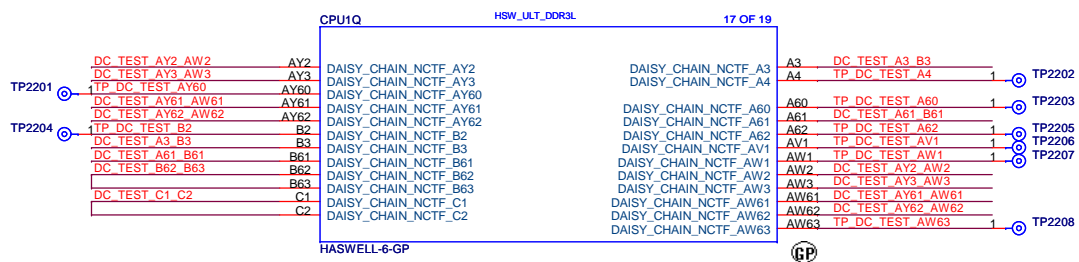
Date Friday June 21 2013

Sheet

of

Rev
X02

SSID = CPU



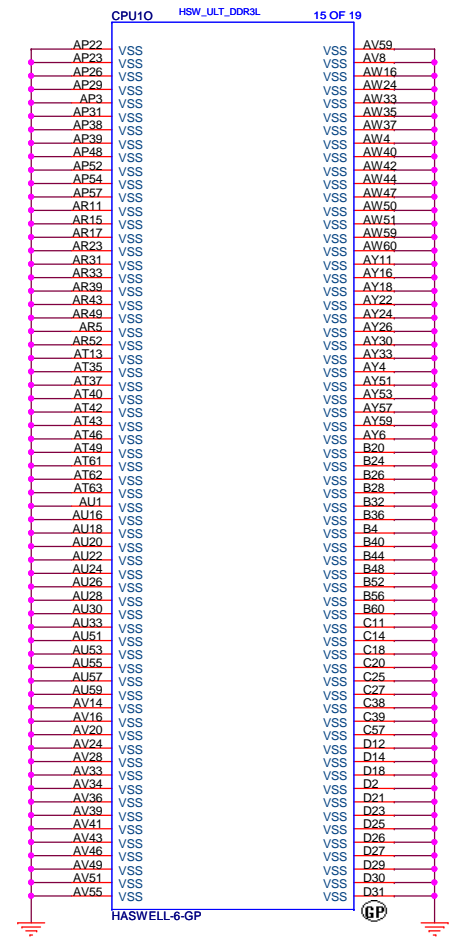
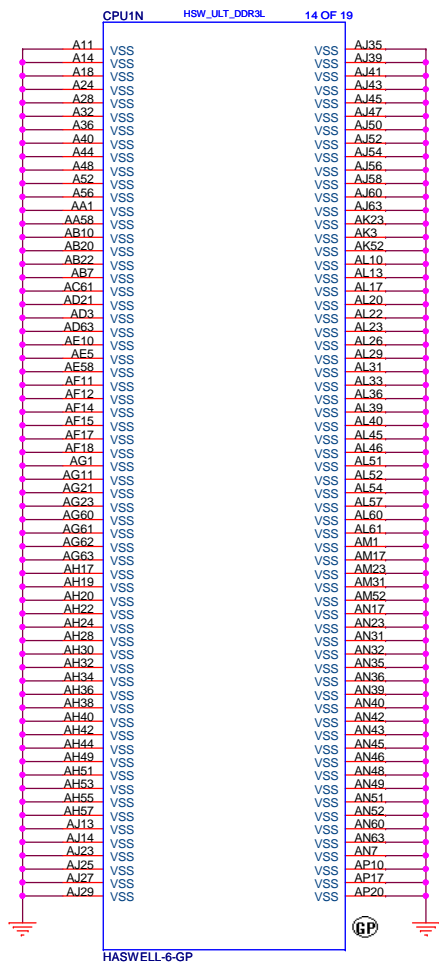
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Title **RSVD**

Size A3	Document Number Hadley 15"	Rev X02
Date Friday, June 21, 2013	Sheet 22	of 101

SSID = CPU



SSID = KBC

Layout Note

Need very close to EC

Layout Note

Need very close to EC

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Layout Note

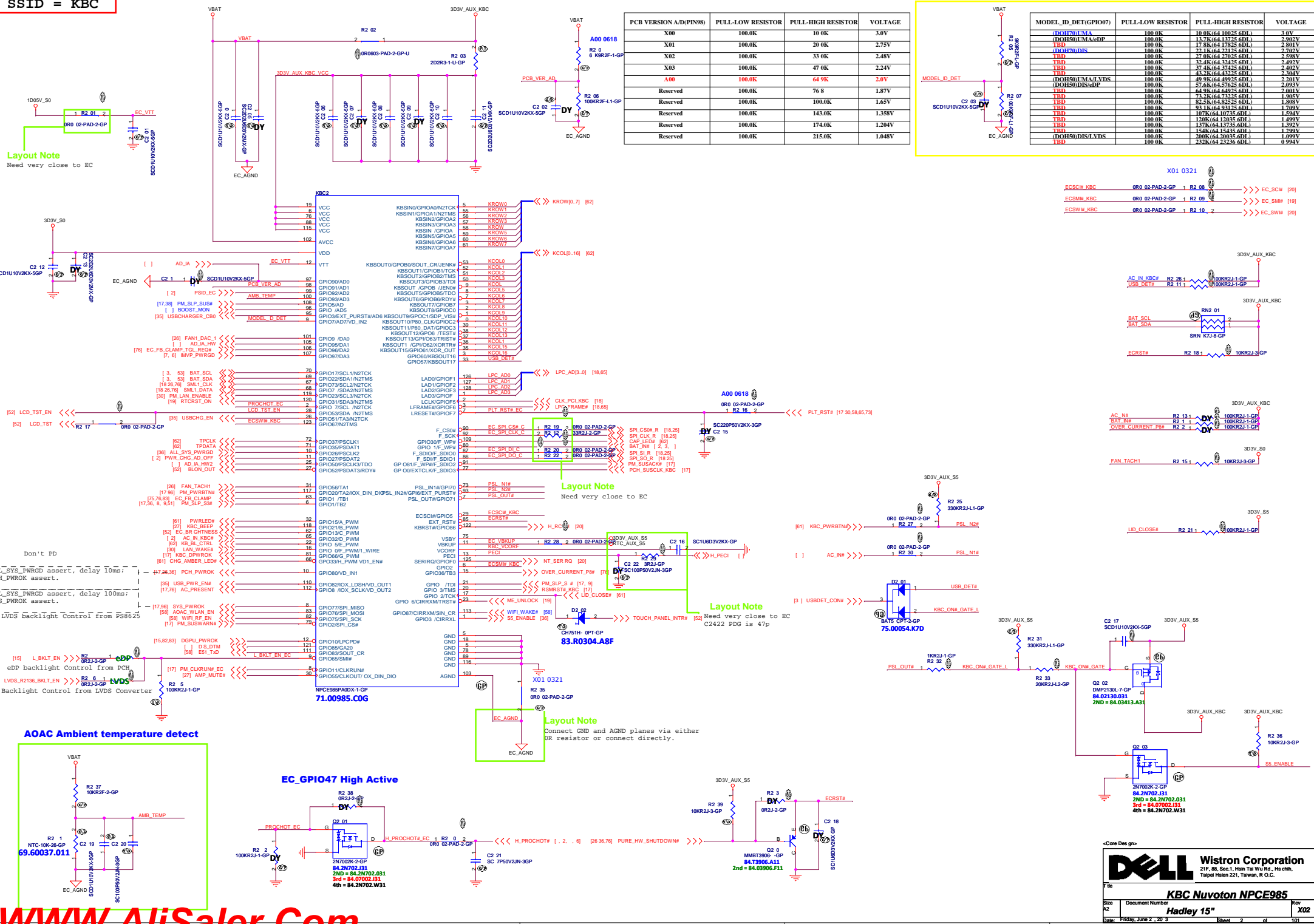
Need very close to EC

Layout Note

Need very close to EC

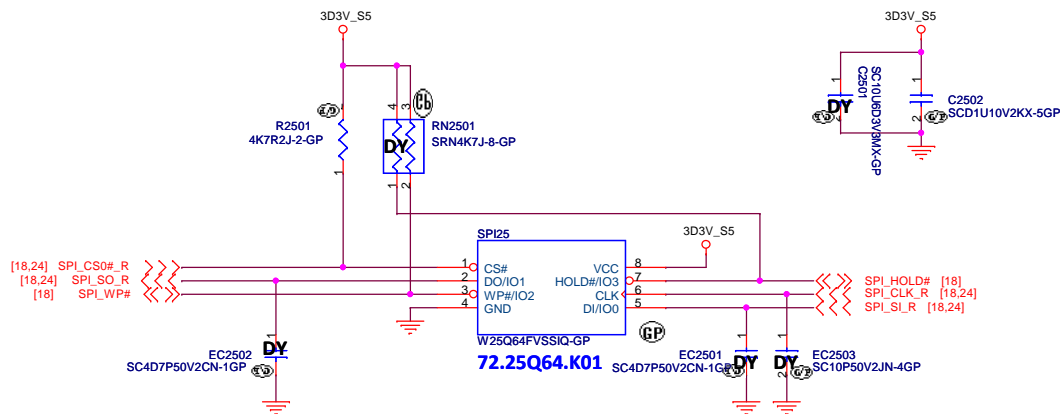
PCB VERSION A/D(PIN#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10 0K	3.0V
X01	100.0K	20 0K	2.75V
X02	100.0K	33 0K	2.48V
X03	100.0K	47 0K	2.24V
A00	100.0K	64 9K	2.0V
Reserved	100.0K	76 8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPI007)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
(DOH50)UMA	100.0K	10.0K(64.10035 6DL)	3.0V
(DOH50)UMA/dP	100.0K	13.7K(64.13735 6DL)	2.902V
(DOH50)DIS	100.0K	17.8K(64.17835 6DL)	2.801V
(DOH50)DIS/dP	100.0K	22.1K(64.22135 6DL)	2.700V
(DOH50)DIS/dP	100.0K	27.0K(64.27035 6DL)	2.598V
(DOH50)DIS/dP	100.0K	32.4K(64.32435 6DL)	2.493V
(DOH50)DIS/dP	100.0K	37.4K(64.37435 6DL)	2.402V
(DOH50)DIS/dP	100.0K	43.2K(64.43235 6DL)	2.304V
(DOH50)DIS/dP	100.0K	49.9K(64.49935 6DL)	2.201V
(DOH50)DIS/dP	100.0K	57.6K(64.57635 6DL)	2.093V
(DOH50)DIS/dP	100.0K	64.9K(64.64935 6DL)	1.985V
(DOH50)DIS/dP	100.0K	82.5K(64.82535 6DL)	1.888V
(DOH50)DIS/dP	100.0K	93.1K(64.93135 6DL)	1.790V
(DOH50)DIS/dP	100.0K	107K(64.10735 6DL)	1.594V
(DOH50)DIS/dP	100.0K	130K(64.13035 6DL)	1.499V
(DOH50)DIS/dP	100.0K	137K(64.13735 6DL)	1.392V
(DOH50)DIS/dP	100.0K	154K(64.15435 6DL)	1.290V
(DOH50)DIS/dP	100.0K	200K(64.20035 6DL)	1.090V
(DOH50)DIS/dP	100.0K	232K(64.23235 6DL)	0.994V



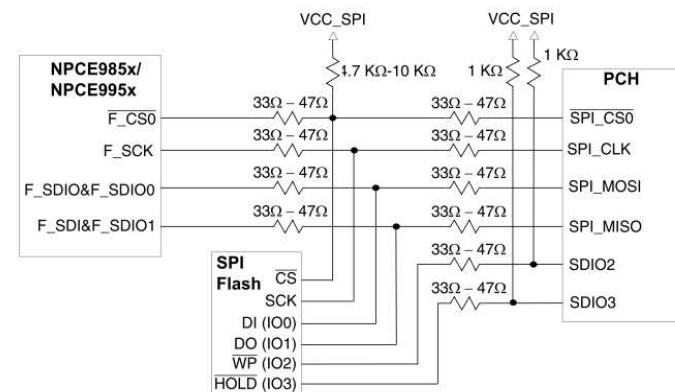
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



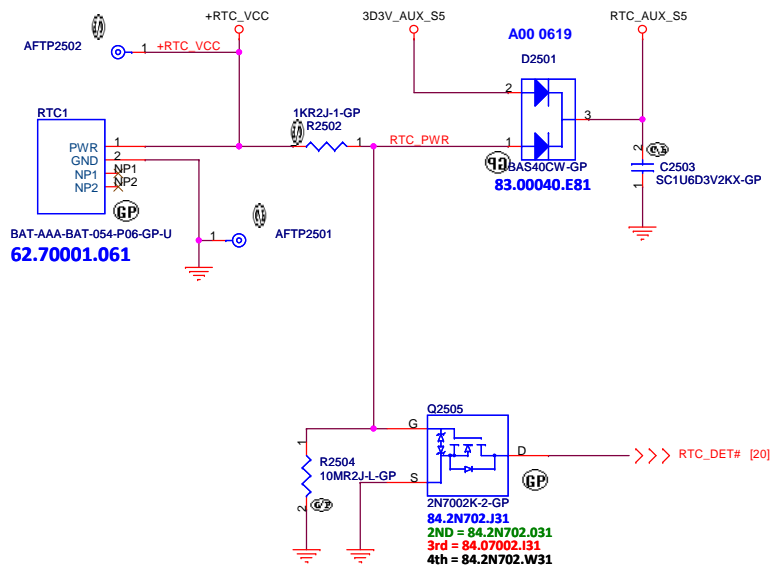
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT



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Flash/RTC

Size

Document Number	
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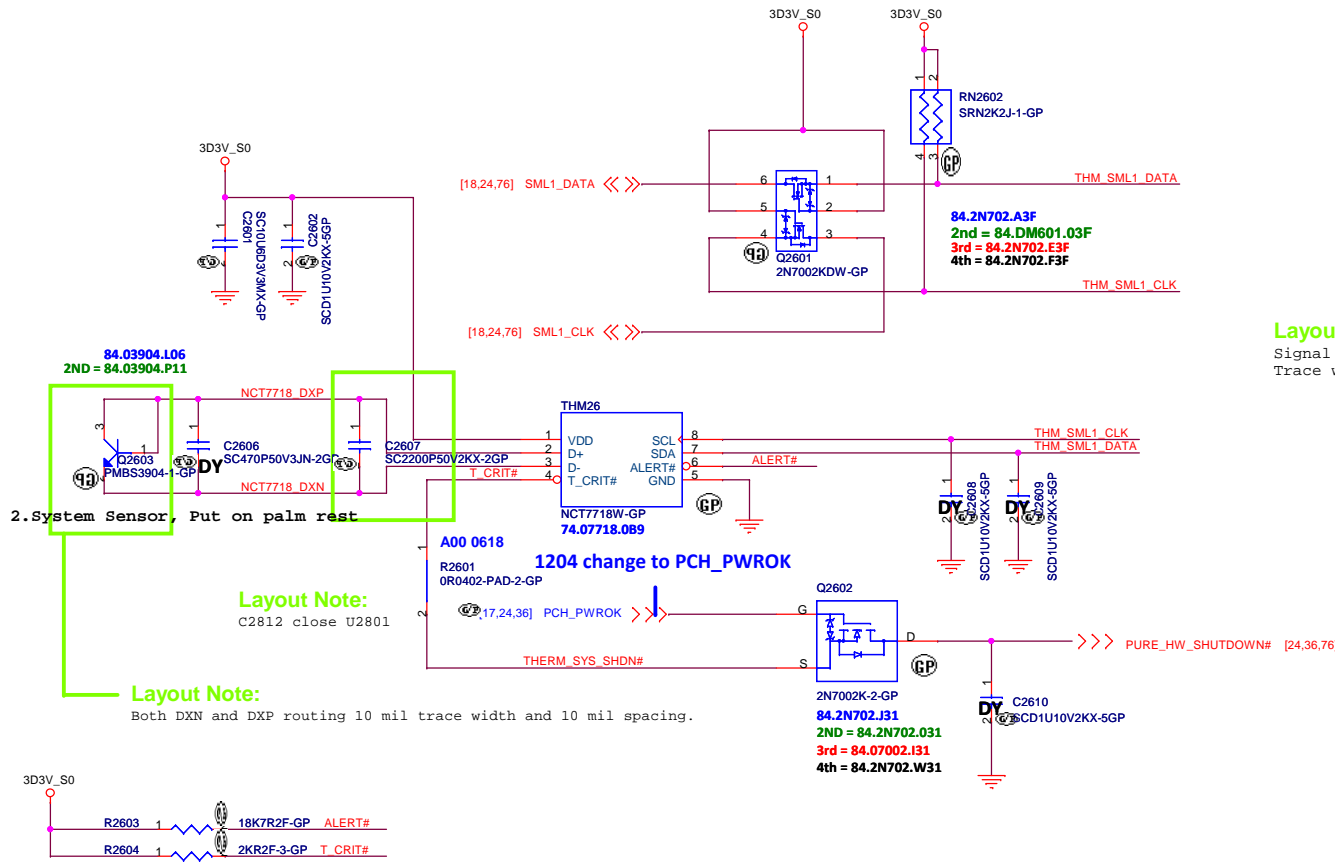
Hadley 15"

Date: Friday, June 21, 2013

Sheet 25 of 101

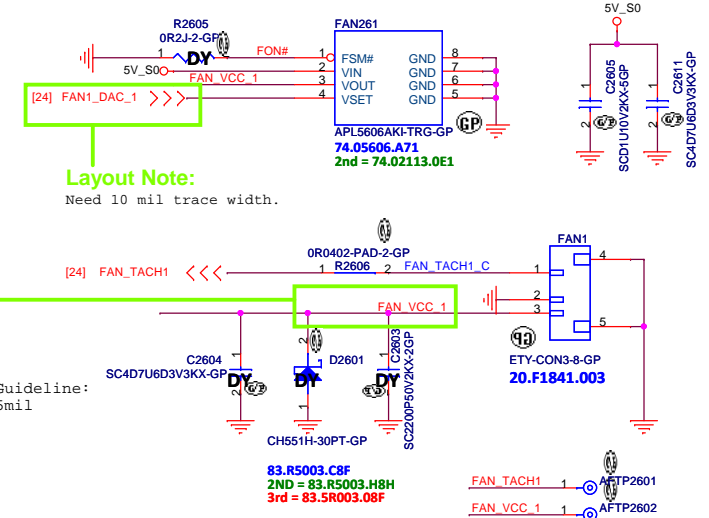
Rev	X02
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SSID = Thermal



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Fan controller1

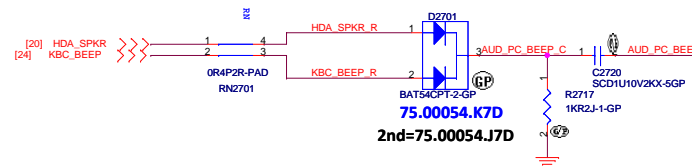
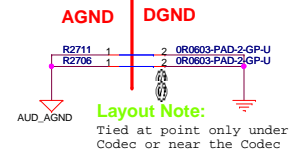
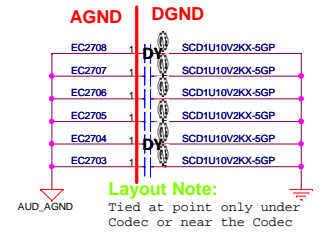
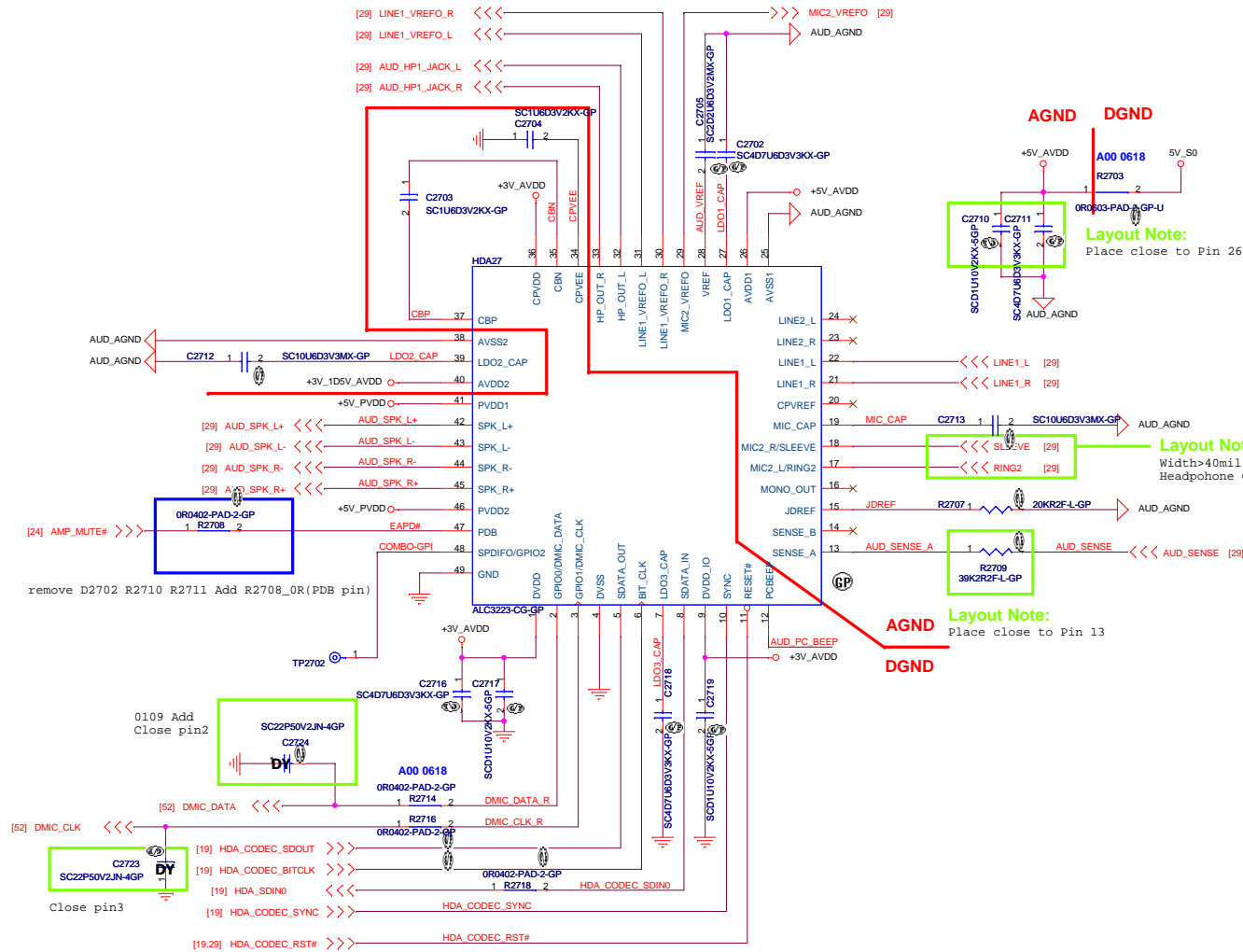
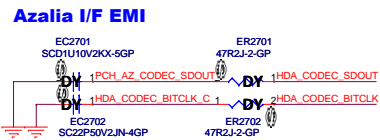
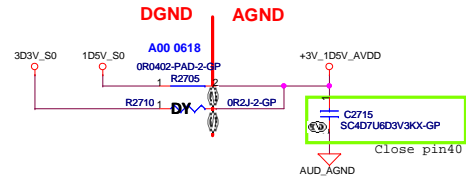
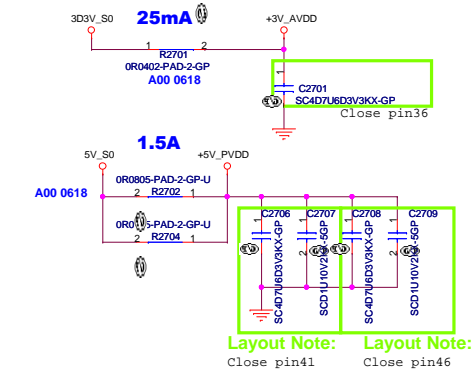


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Title
Thermal NCT7718W/Fan
Size A3 Document Number
Hadley 15" Rev
X02
Date Friday, June 21, 2013 Sheet 26 of 101

SSID = AUDIO



(Blanking)

<Core Design>



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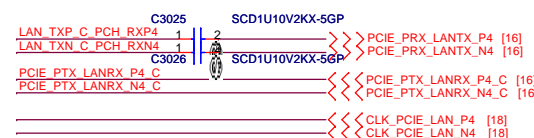
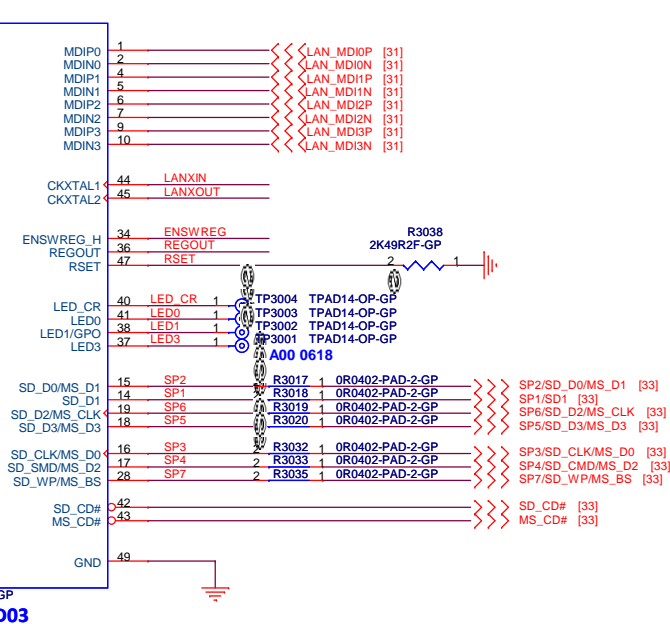
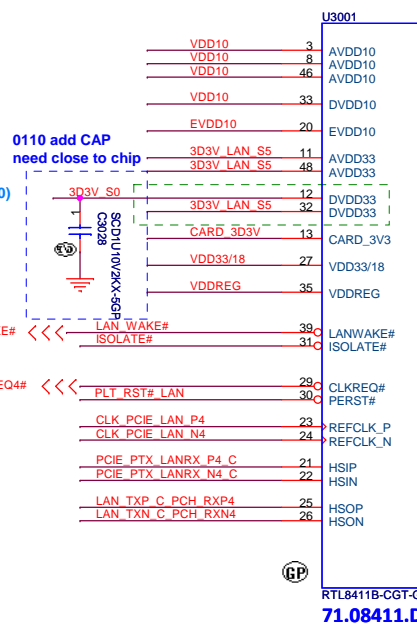
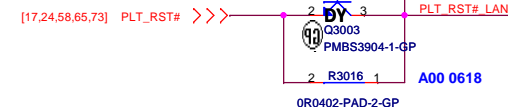
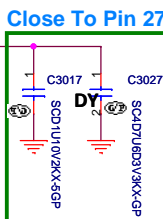
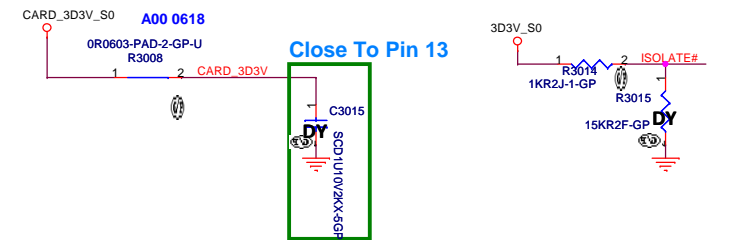
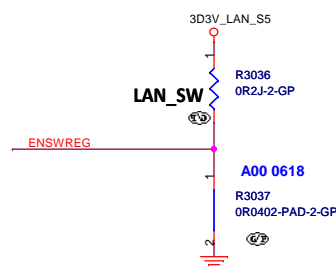
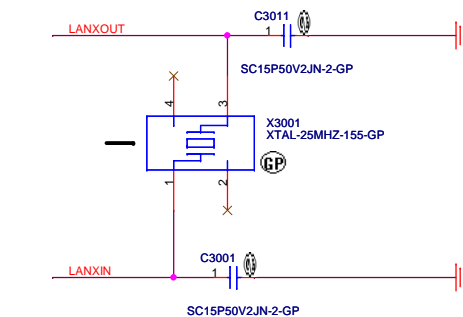
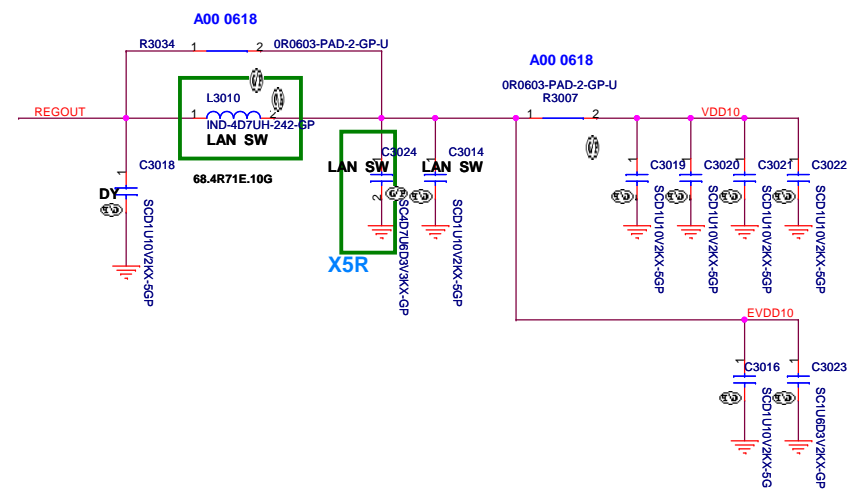
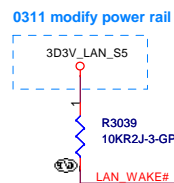
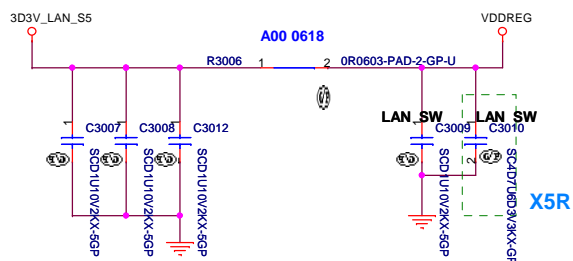
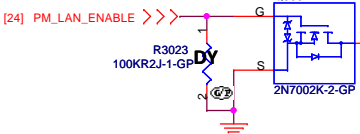
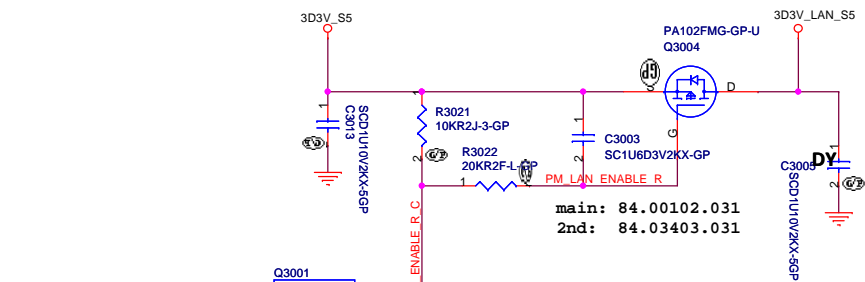
Title

Reserved

Size	Document Number	Rev
A3	Hadley 15"	X02

Date	Friday, June 21, 2013	Sheet	28	of	101
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SSID = LOM



<Core Design>



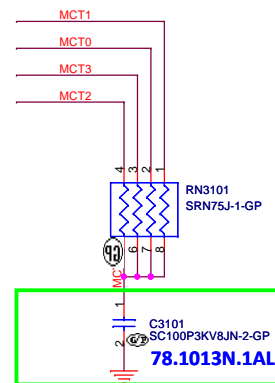
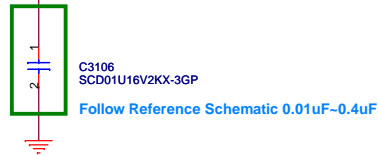
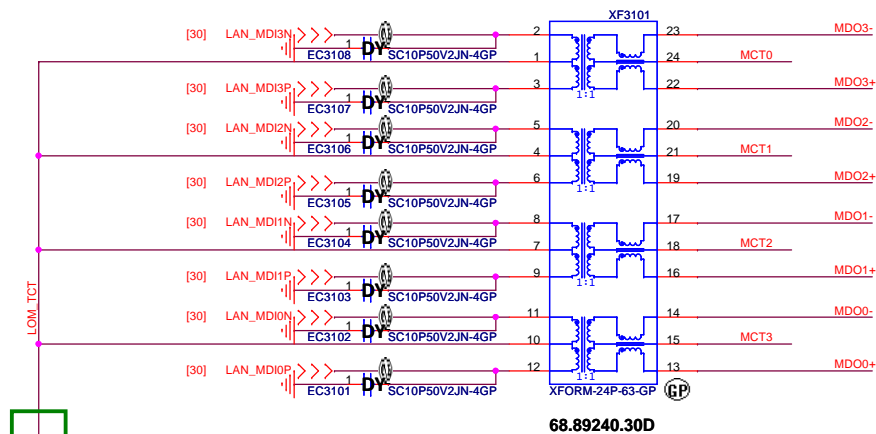
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Title			
LOM(RTL8411B)			
Size A3	Document Number		Rev
	Hadley 15"		X02
Date	Friday, June 21, 2013	Sheet 30 of	101

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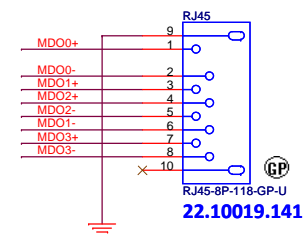
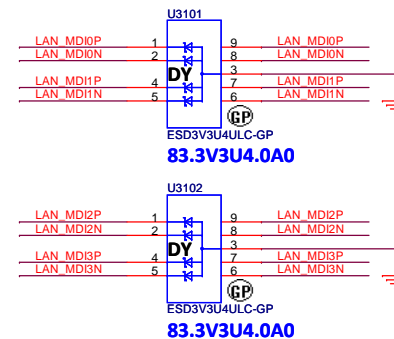
SSID = LOM

GIGA LAN Transformer



Layout:
Place near RJ45

AFTP3107	1	MDO0+
AFTP3102	1	MDO0-
AFTP3101	1	MDO1+
AFTP3103	1	MDO2+
AFTP3104	1	MDO2-
AFTP3106	1	MDO1-
AFTP3105	1	MDO3+
AFTP3108	1	MDO3-



<Core Design>



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Title

RJ45+Transformer

Size

A3

Document Number

Hadley 15"

Rev


X02

Date Friday, June 21, 2013

Sheet 31 of 101

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<Core Design>



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Title

Reserved

Size
A3

Document Number
Hadley 15"

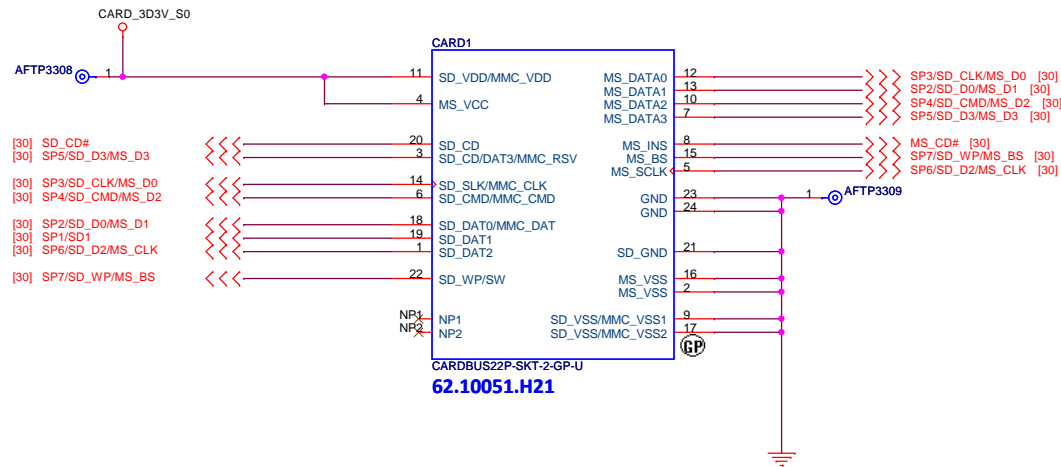
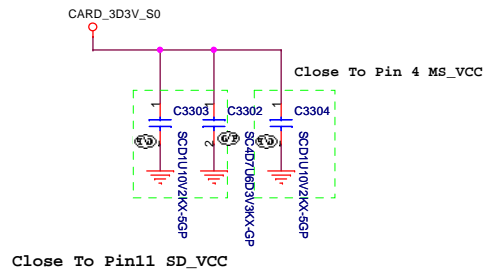
Rev
X02

Date
Friday, June 21, 2013

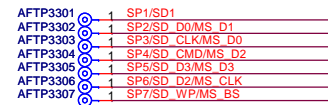
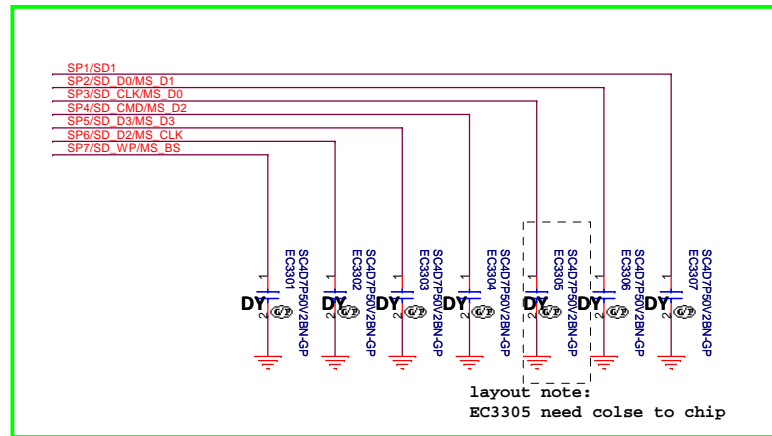
Sheet
32

of
101

SSID = SDIO



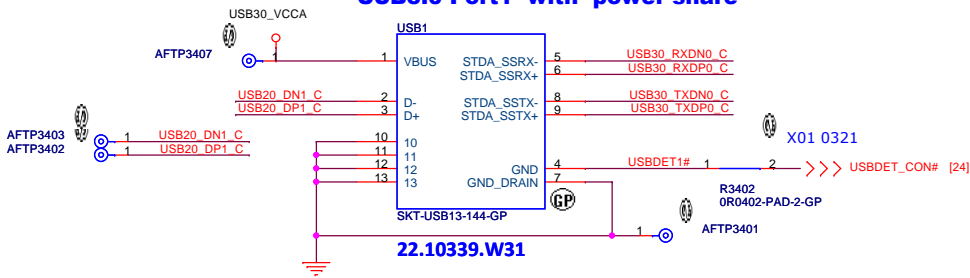
Reserve EMI Cap, 0107 CLK Cap DY



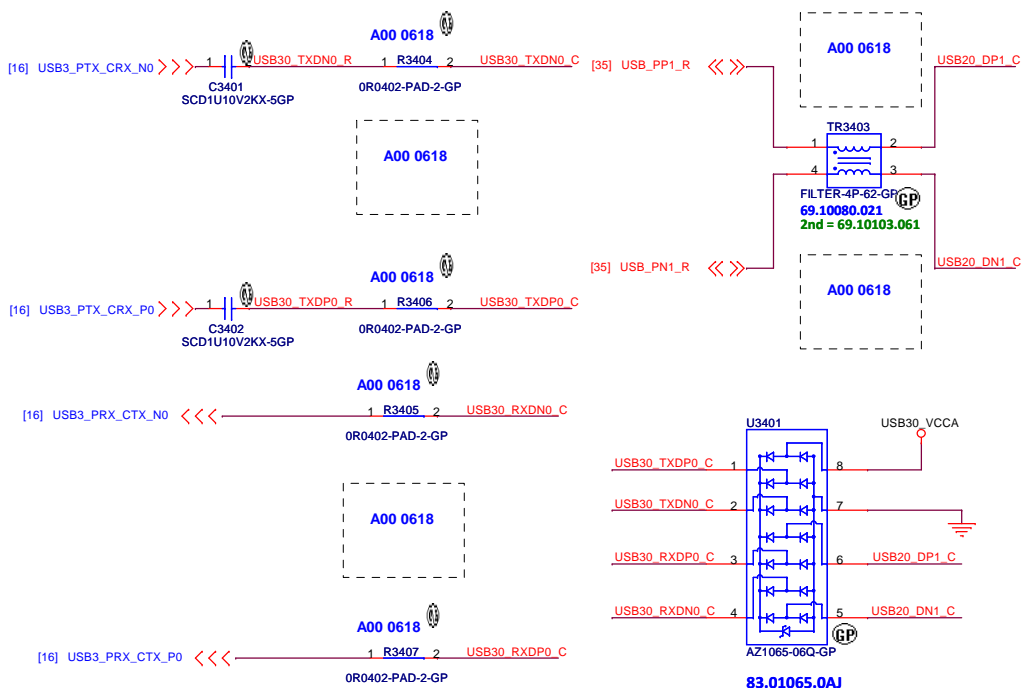
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SSID = USB

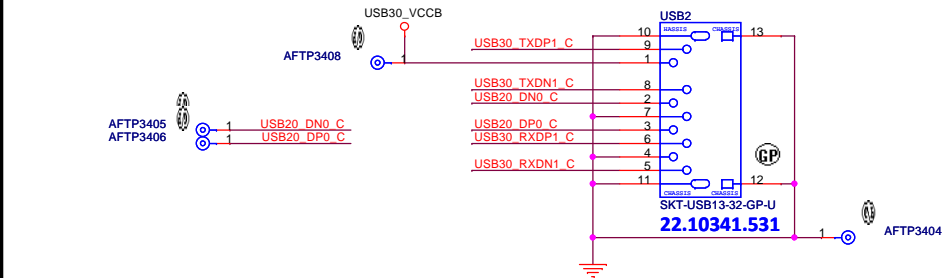
USB3.0 Port1 with power share



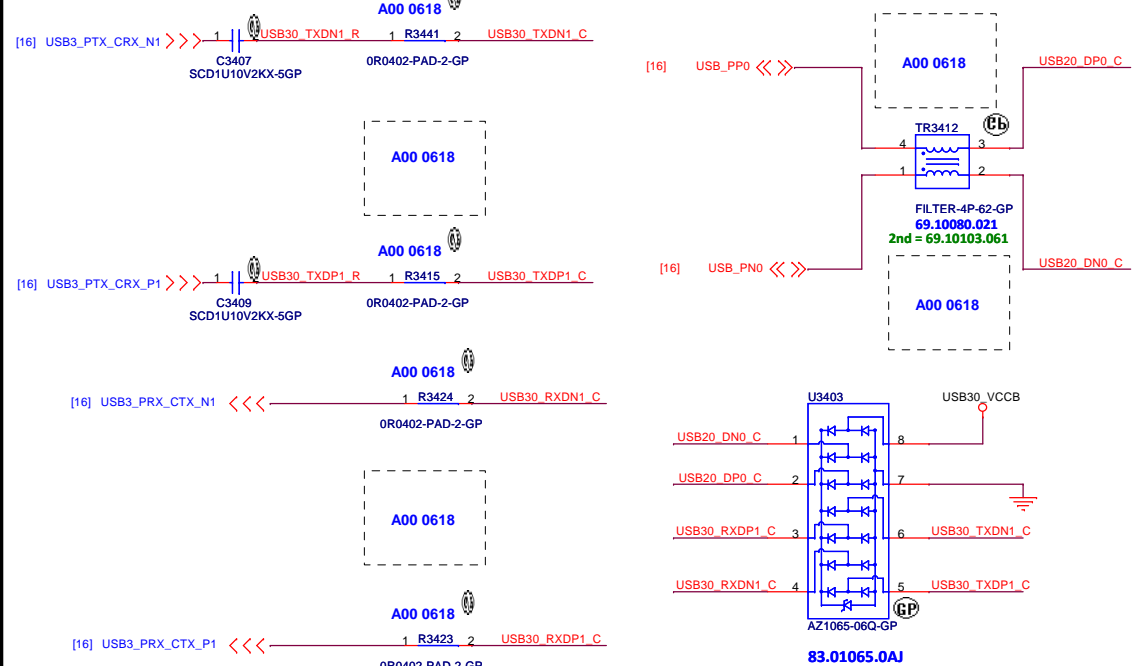
X02 stuff TR3403



USB3.0 Port2



X02 stuff TR3412



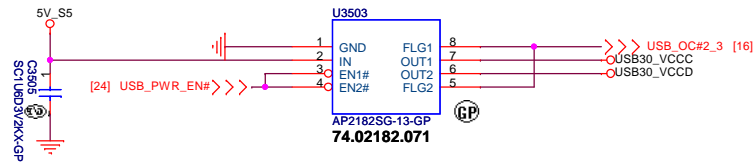
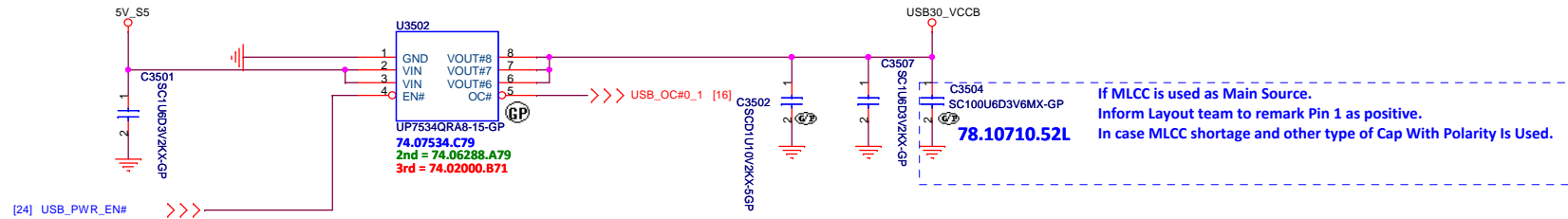
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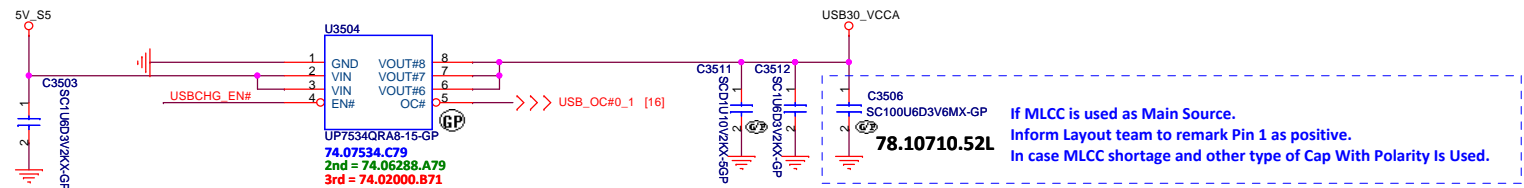
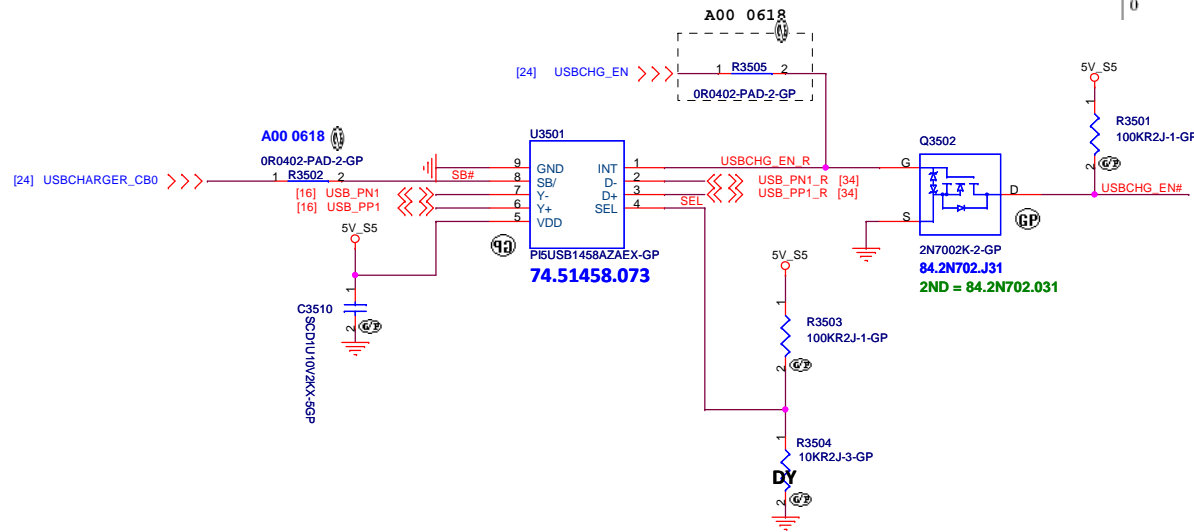
Title			USB3.0(1)		
Size	Document Number	Rev			
A3	Hadley 15"	X02			
Date	Friday, June 21, 2013	Sheet	34	of	101

SSID = USB



0319 modify USB Charger circuit

SB/ (pin 8)	SEL(pin 4)	Feature	pin 1 role (INT or INT/)
0	0	Auto S & C without mouse/keyboard pass through	INT or INT/
0	1	Auto S & C with mouse/keyboard pass through	INT or INT/
1	0	S0 charging with SDP only	INT or INT/
1	1	S0 charging with CDP or SDP only (depending on external device)	INT or INT/
0	M = (1/2)*V _{DD}	Test Mode, M = V _{DD} /2 = (1/2)*V _{DD}	



USB Power SW (U3504)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.071	2ND
GMT	G547I2P81U	74.00547.F79	3RD

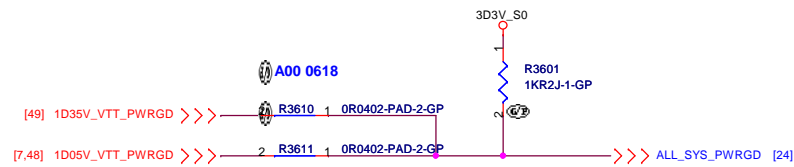
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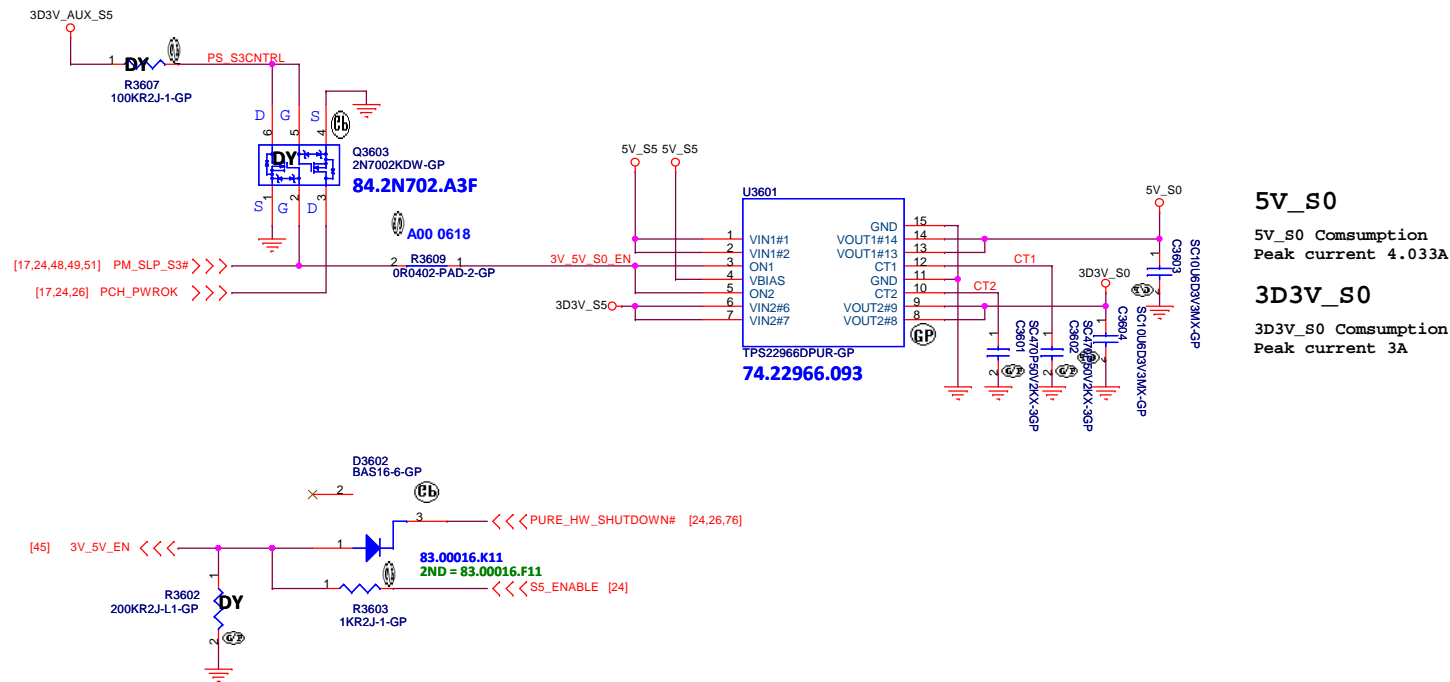
Title			USB Power SW
Size	Document Number	Rev	X02
Date	Friday, June 21, 2013	Sheet	35 of 101

SSID = Reset.Suspend

Power Good



ROSA Run Power



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Power Plane Enable			
Size	Document Number	Rev	
A3		Hadley 15" X02	
Date	Friday, June 21, 2013	Sheet	36 of 101

SSID = Reset.Suspend

Layout Note:

Place Close SO-DIMMA.

SA_DIMM_VREFDQ
SODIMM1

M_VREF_CA_DIMMA

SB_DIMM_VREFDQ
SODIMM2

M_VREF_CA_DIMMB

0D675V_VTTREF

0R2J-2-GP
R3704

1D35V_S3

R3706
1K8R2F-GP

2R2F-GP
R3708

R3703
1K8R2F-GP

R3705
0R0402-PAD-2-GP

C3701
SCD022U16V2JX-GP

+V_VREF_PATH3

R3707
24D9R2F-L-GP

Close to DIMM
S3 Power Reduction Circuit PM DRAM PWRGD

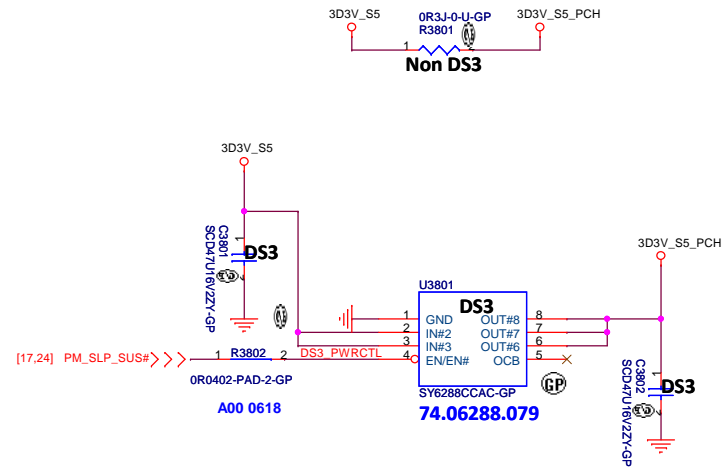
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Title			S3 Power Reduction	
Size	Document Number	Hadley 15"		Rev
A3				X02
Date	Friday, June 21, 2013	Sheet	37	of 101

```
SSID = Reset.Suspend
```



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Title

DSW

Size
A3

Document Number

Hadley 15"

Rev


X02

Date Friday, June 21, 2013

Sheet 38 of 101

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<Core Design>



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Title

Reserved

Size
A3

Document Number
Hadley 15"

Rev
X02


Date
Friday, June 21, 2013

Sheet
39

of
101

(Blanking)

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Title

Reserved

Size
A3

Document Number
Hadley 15"

Rev
X02


Date
Friday, June 21, 2013

Sheet
40

of
101

(Blanking)

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Title

Reserved

Size

A3

Document Number

Hadley 15"

Rev

X02

Date

Friday, June 21, 2013

Sheet

41

 of

101

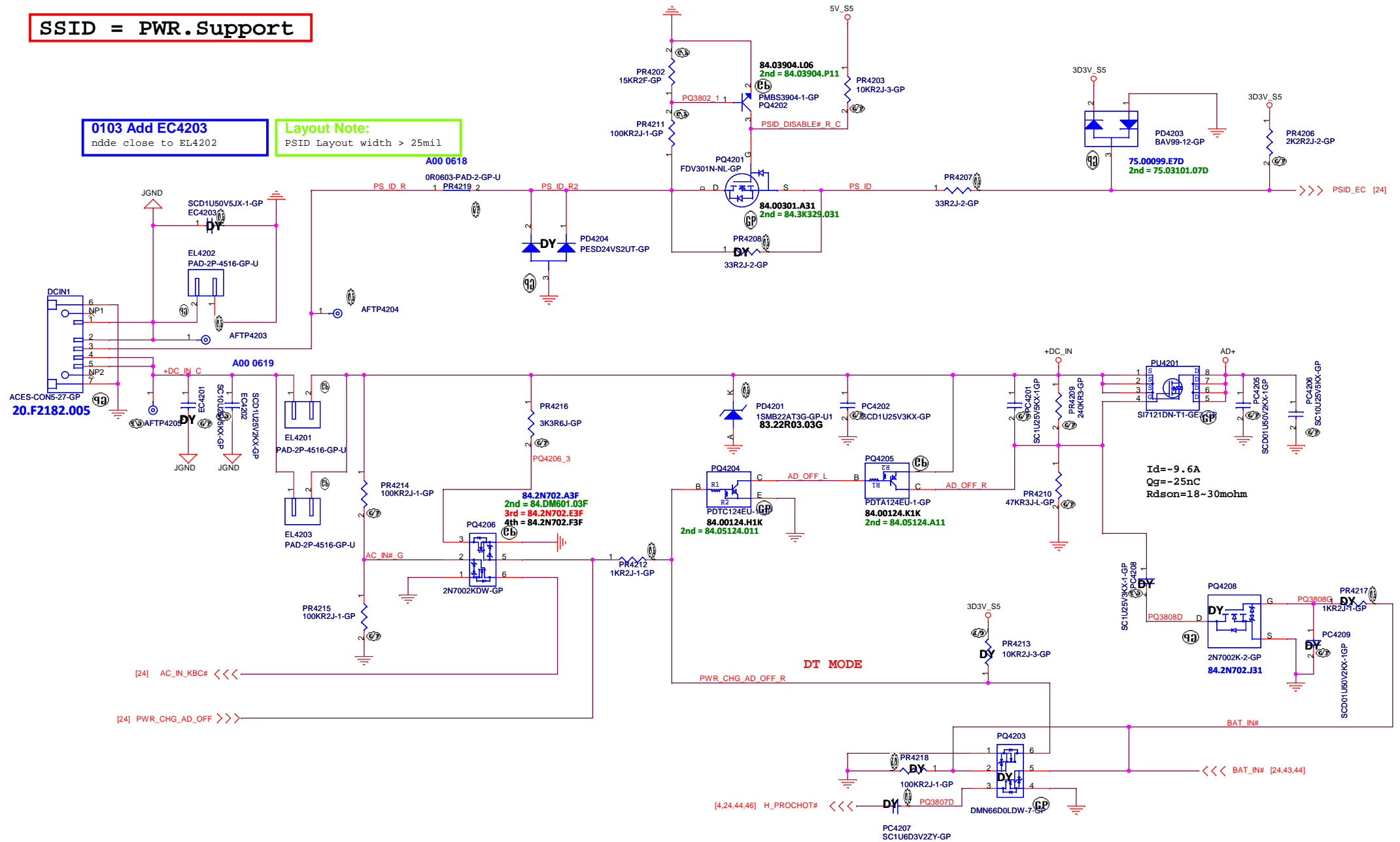
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0103 Add EC4203

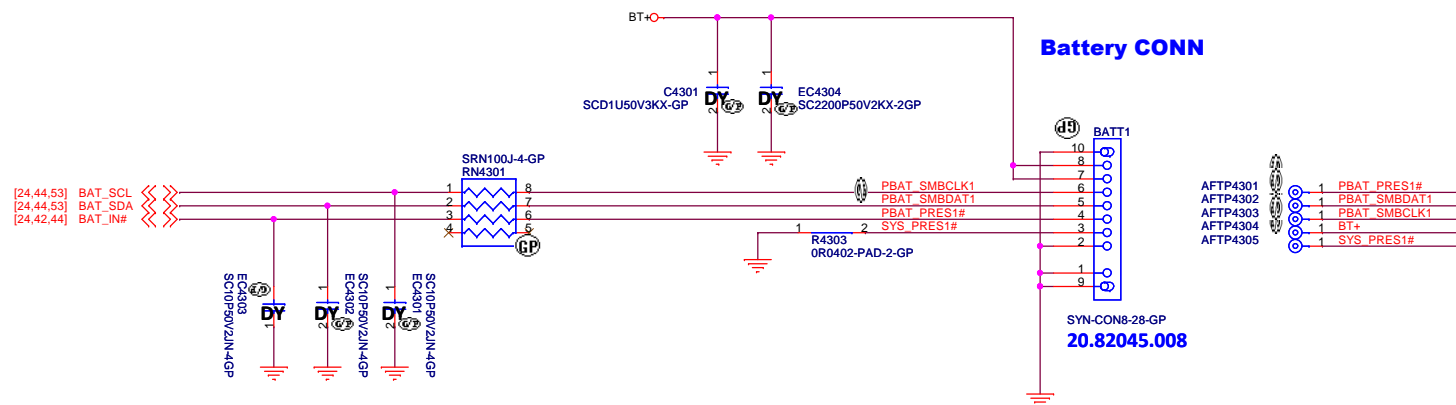
ndde close to EL4202

Layout Note:

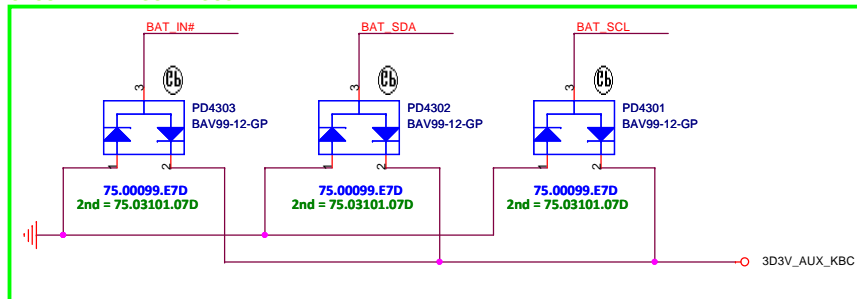
PSID Layout width > 25mil



SSID = PWR.Support



0109 DY PD4301~4303



Layout Note:

Place near Battery CONN

<Core Design>



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Title			BATT CONN		
Size	Document Number	Rev			
A3	Hadley 15"	X02			
Date	Friday, June 21, 2013	Sheet	43	of	101

SSID = Charger

KBC FOR DT MODE
CHECK EE PULL HIGH

DIS DTM:
H= cell is plus to GND. (reset charger ic)
L=normal

Follow customer circuits

Follow customer circuits

CHECK EE

BATTERY MON

Close PR4443

CHECK PM BATTERY TYPE
CHECK CELL for DT mode

CHECK PM ADAPTER TYPE
And setting adapter type

(AD_IA_HW)

ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329V
45W	L	H	0.659648V

Core Design:

DELL Wistron Corporation
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Taichung Hsien 221, Taiwan, R.O.C.

File **CHARGE(BQ24715)**

Rev 1.0

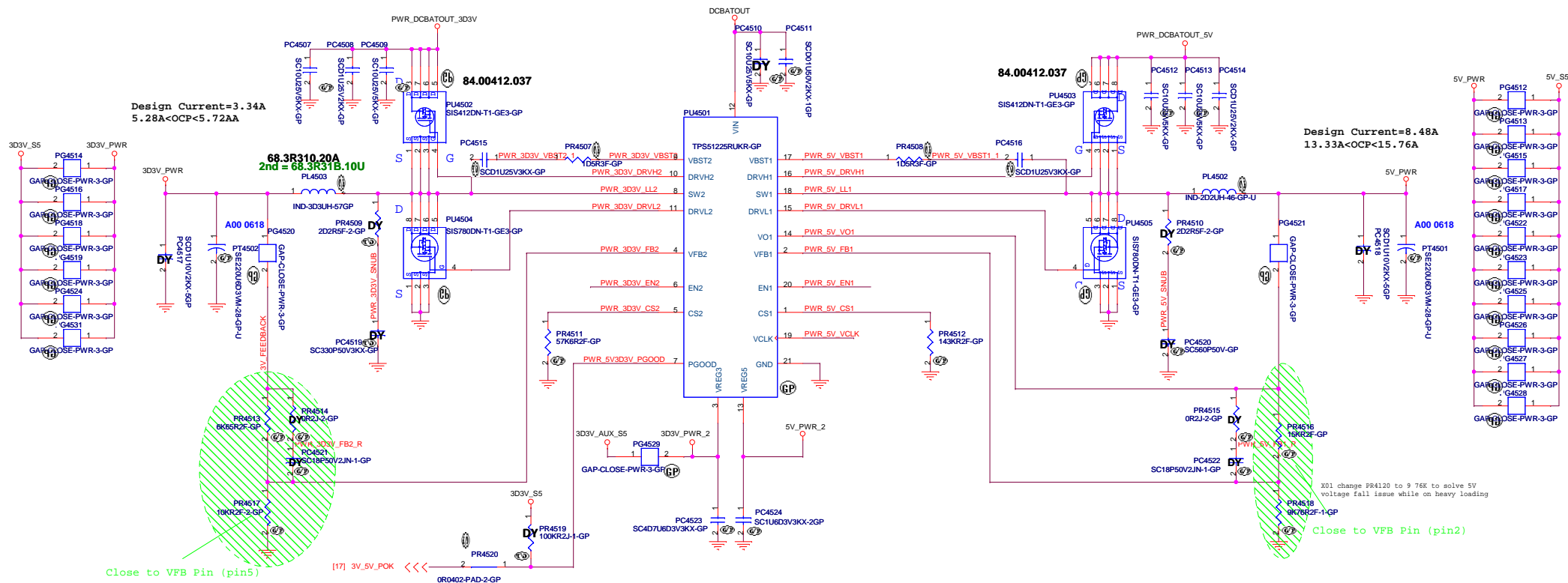
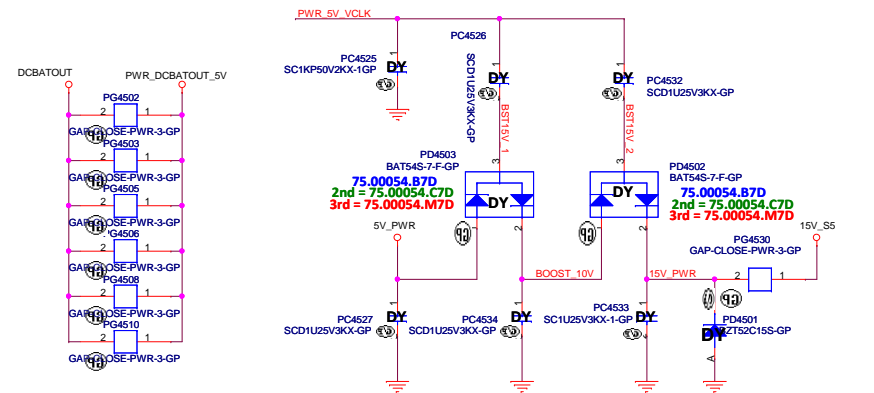
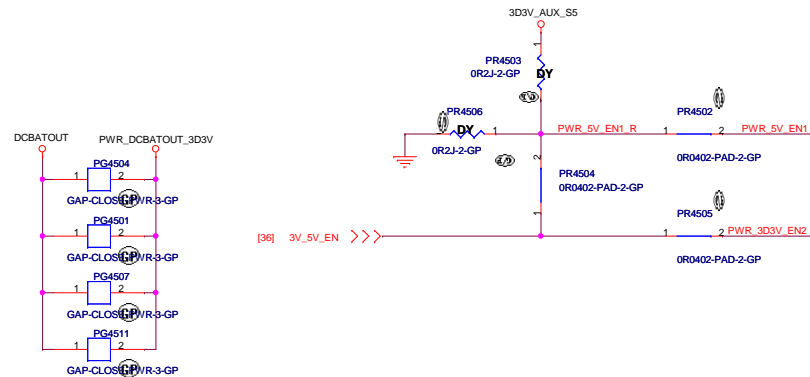
Document Number

Rev 1.0

Date: Friday, June 21, 2013

Sheet 1 of 1

```
SSID = PWR.Plane.Regulator_5v3p3v
```



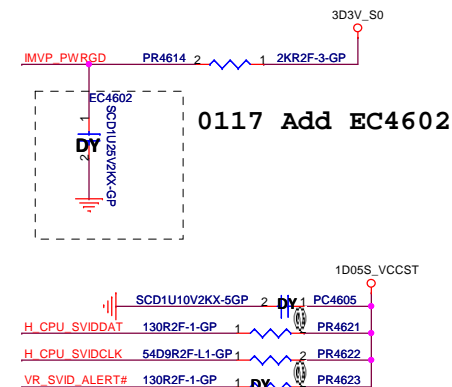
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Title			
3V/5V TPS51225			
Size	Document Number	Rev	
Cust m	Hadley 15"	X02	
Date	Friday, June 21, 2013	Sheet 45 of	101

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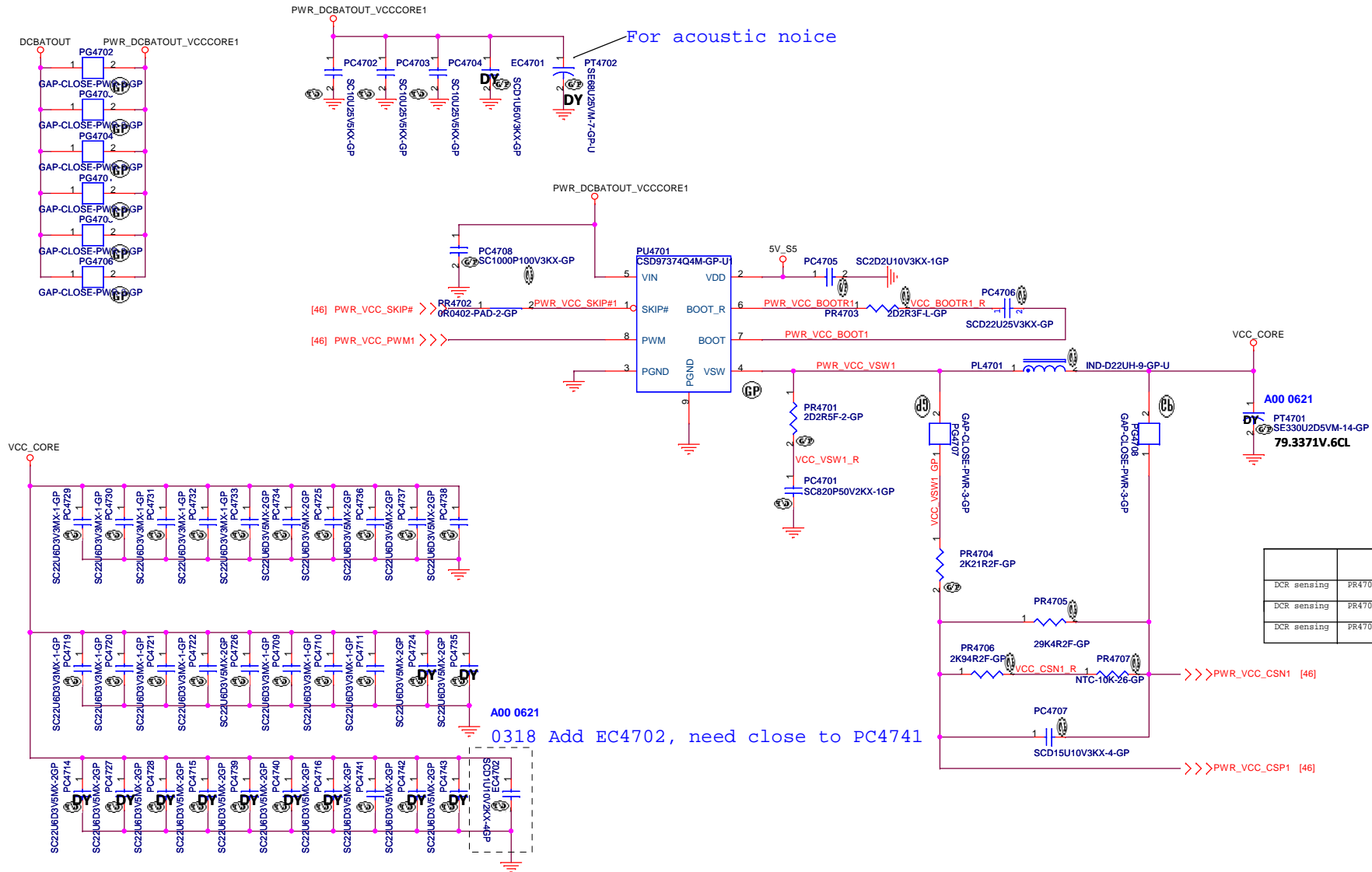
		28W	15W
F5w	PR4604	392K	1M
F5w	PR4607	75K	150K
OCp	PR4609	150k	75K
IMON	PR4610	680K	422K
Load line	PR4620	2.8K	3K

DELL

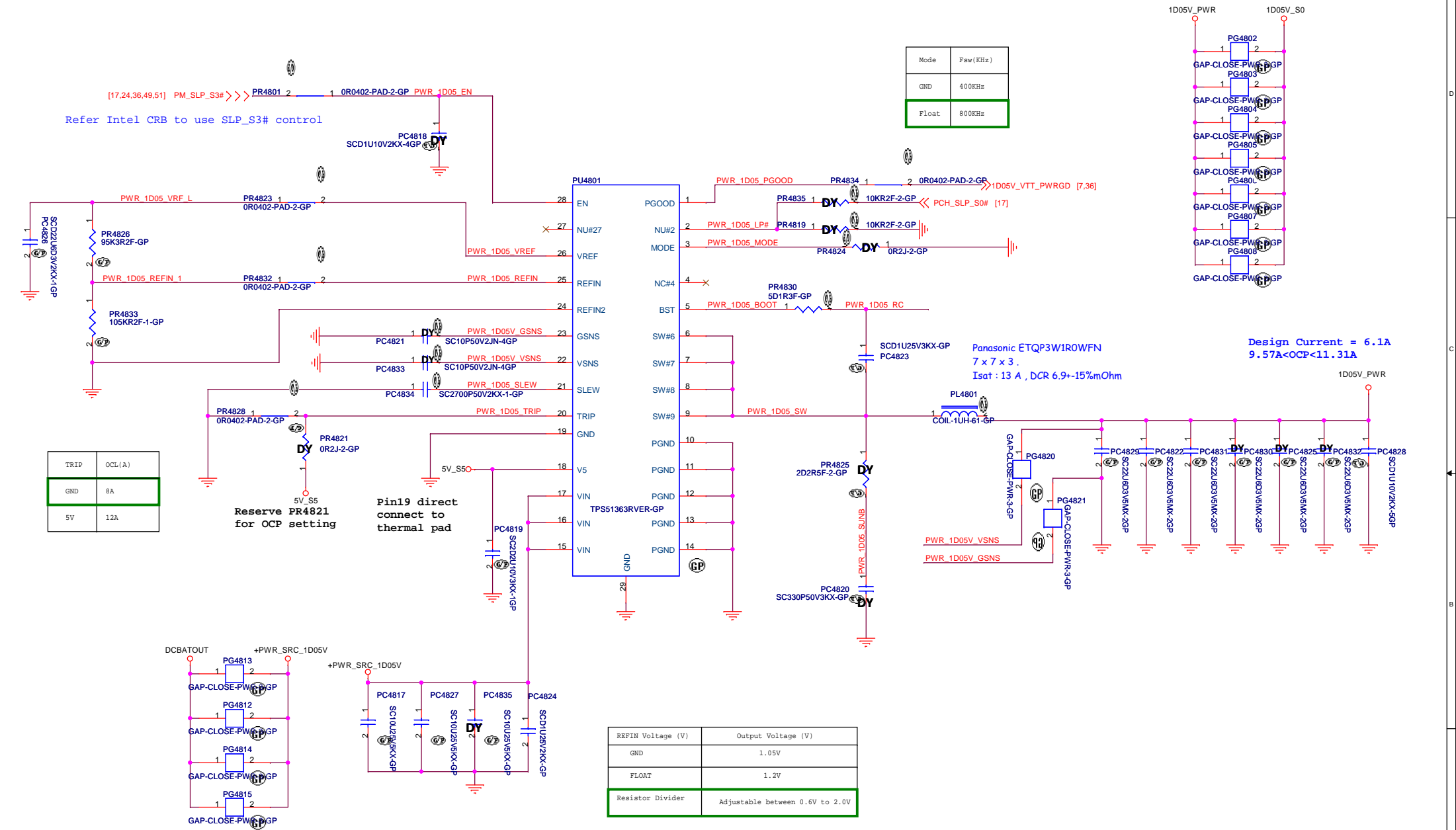
Title	TPS51622 CPUCORE(1/2)
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Sheet 46 of 101

SSID = CPU.Regulator




SSID = PWR.Plane.Regulator_1p05v



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I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 1.0UH ETQP3W1R0WFN / Panasonic/ 6.9mOhm / Isat =13Arms/ 68.1R01D.20H
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R /78.22610.51L

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File			TPS51363 1D05V		
Size	Document Number	Rev			
A3		Hadley 15"		X02	
Date	Friday, June 21, 2013	Sheet	48	of	101

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	



T the

TPS51216 +1.35V SUS

Size

Document Number

Hadley 15"

Date _____

Friday, June 21, 2013

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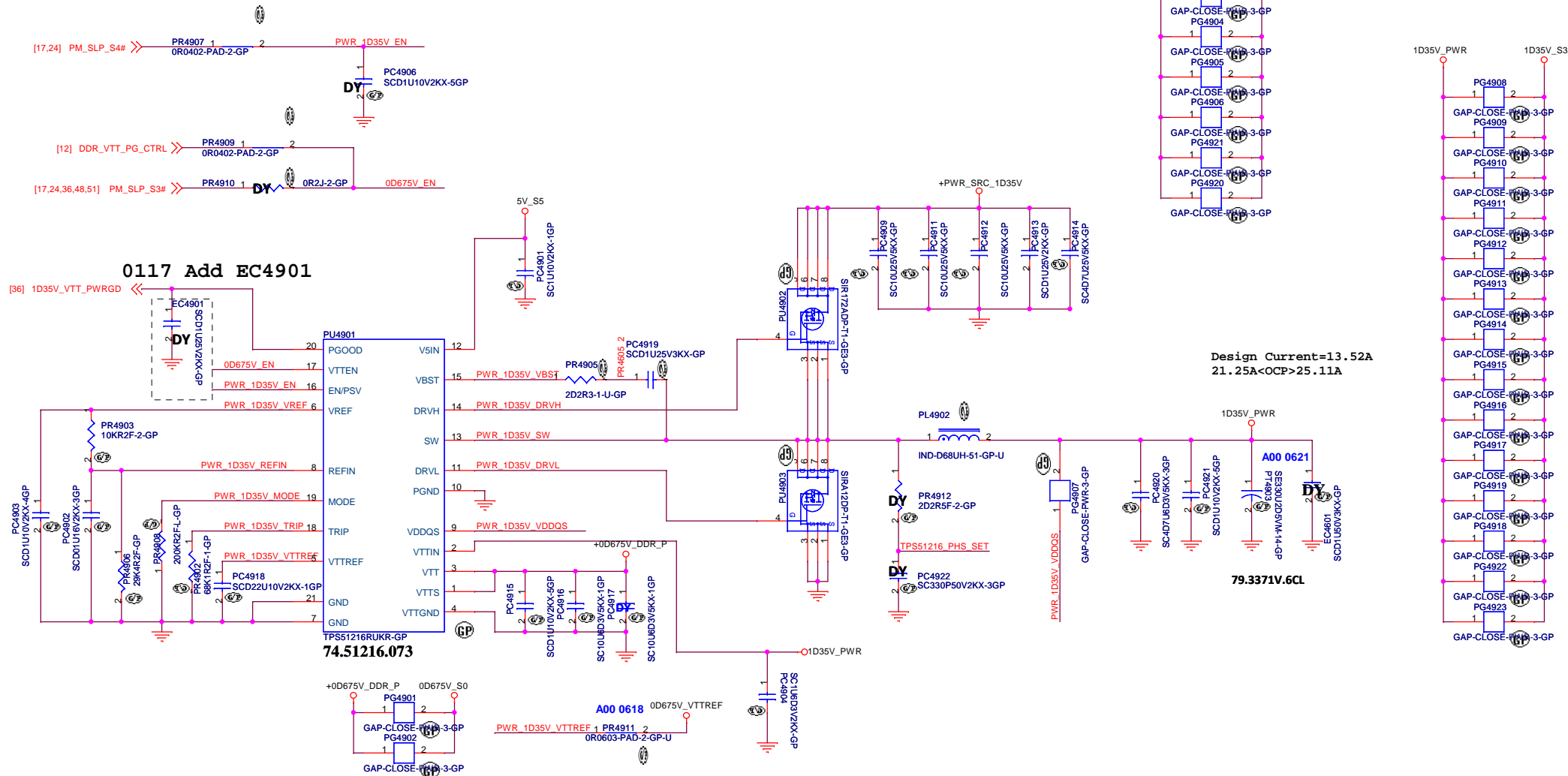
49

of

Rev


x

101



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Taipei Hsien 221, Taiwan, R.O.C.

File

(Reserved)TPS51312 1D8V

Size
A3

Document Number
Hadley 15"

Rev
X02

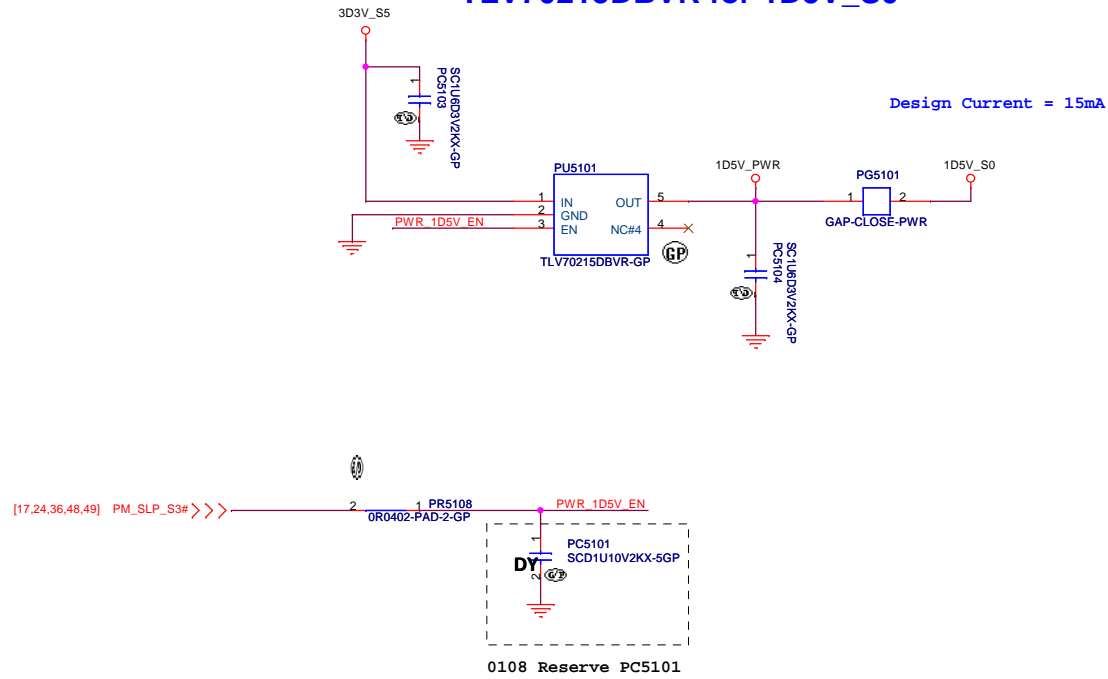
Date
Friday, June 21, 2013

Sheet
50

of
101

```
SSID = PWR.Plane.Regulator_1p5v
```

TLV70215DBVR for 1D5V_S0



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T	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t
T	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t

RT9198-15PU5R_1D5V

Size
A3

Document Number

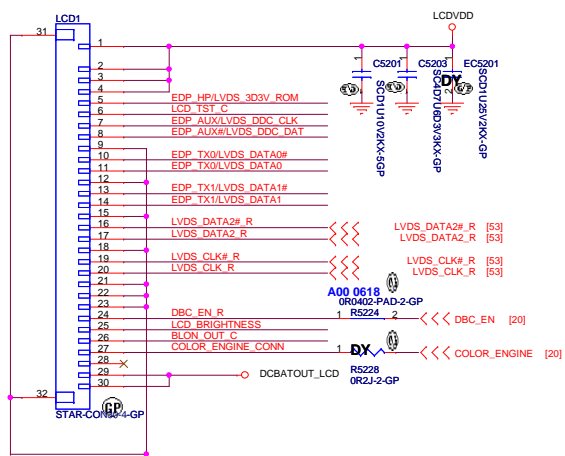
Hadley 15"

Rev
X02

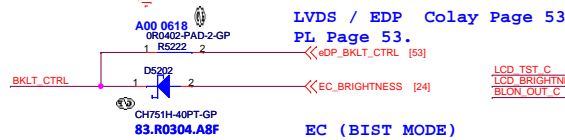
Date Friday, June 21, 2013

Sheet 51 of 101

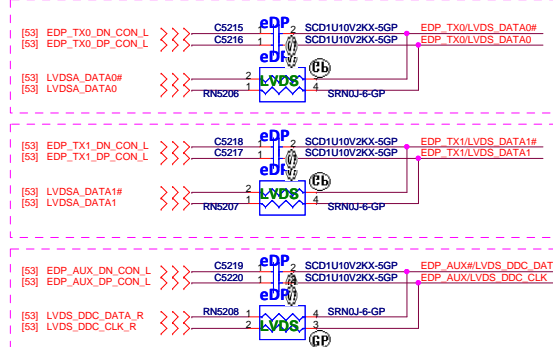
SSID = VIDEO



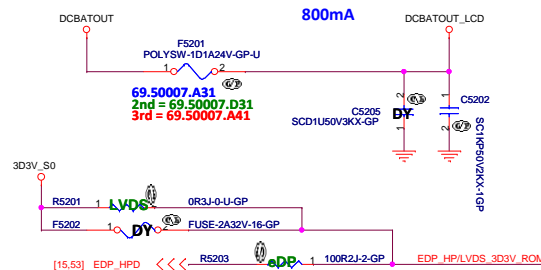
Pin	eDP	LVDS	Pin	eDP	LVDS
1	LCDVDD	LCDVDD	16	NC	LVDS_DATA2
2	LCDVDD	LCDVDD	17	NC	LVDS_DATA2
3	LCDVDD	LCDVDD	18	GND	GND
4	LCDVDD	LCDVDD	19	NC	LVDS_CLK#_1
5	EDP_HP	3D3V_ROM	20	NC	LVDS_CLK_R
6	LCD_TST_C	LCD_TST_C	21	GND	GND
7	EDP_AUX	LVDS_DDC_CLK	22	GND	GND
8	EDP_AUX#	LVDS_DDC_DAT	23	GND	GND
9	GND	GND	24	DBC_EN	DBC_EN
10	EDP_TX0N	LVDS_DATA0#	25	BRIGHTNESS	BRIGHTNESS
11	EDP_TX0P	LVDS_DATA0	26	BLON_OUT	BLON_OUT
12	GND	GND	27	Color_Engine	Color_Engine
13	EDP_TX1N	LVDS_DATA1#	28	NC	NC
14	EDP_TX1P	LVDS_DATA1	29	DCBATOUT_LCD	DCBATOUT_LCD
15	GND	GND	30	DCBATOUT_LCD	DCBATOUT_LCD



eDP/ LVDS select circuit

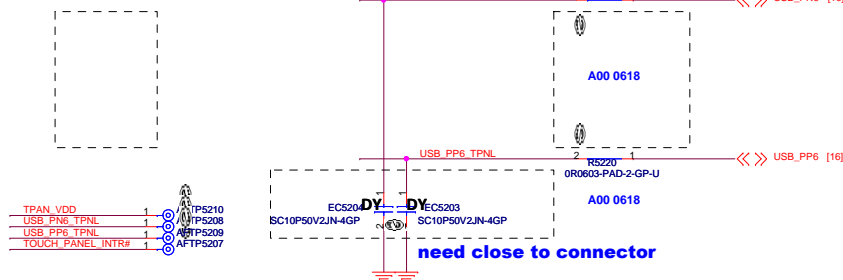


INVERTER POWER

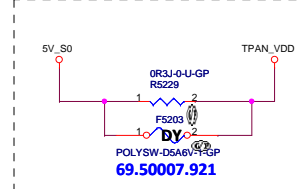


Touch panel

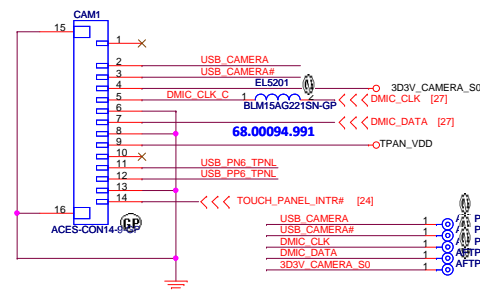
X02 remove TPNL1



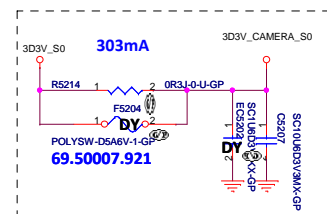
0307 modify



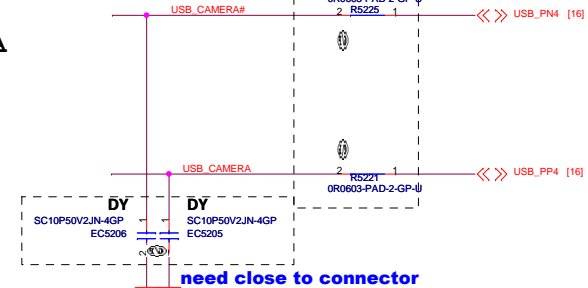
X02 change CAM1 connector



Camera Power

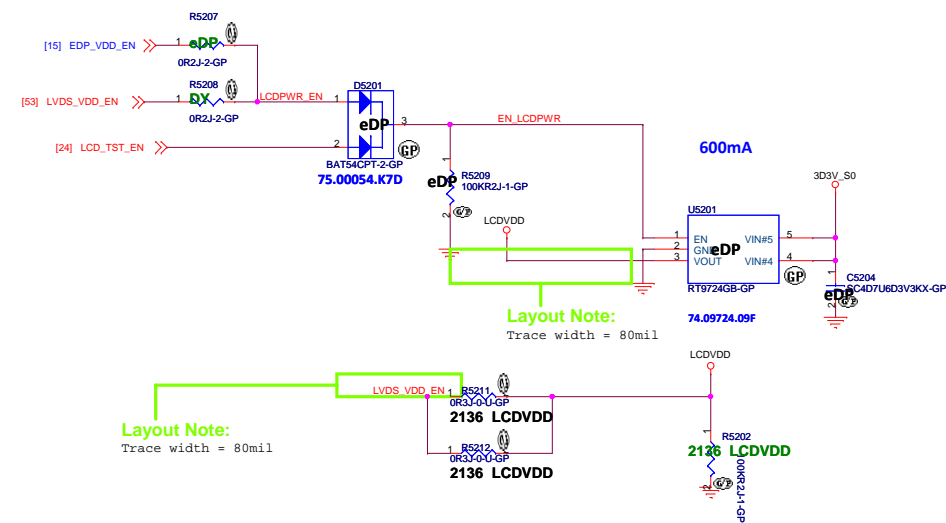


CAMERA



LCDVDD

LCD Power



<Core Design>



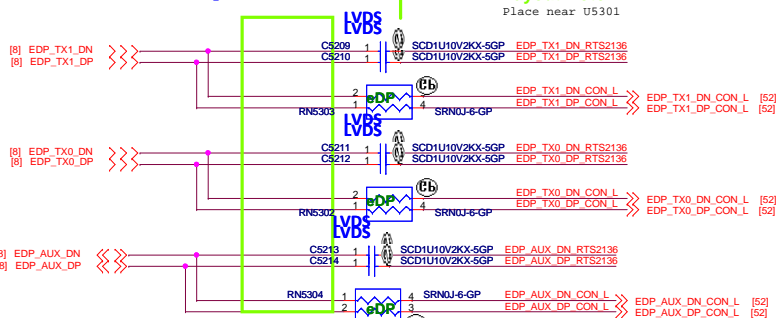
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Title			
LCD Connector			
Size Custom	Document Number	Rev	
	Hadley 15"	X02	
Date	Friday, June 21, 2013	Sheet 52	of 101

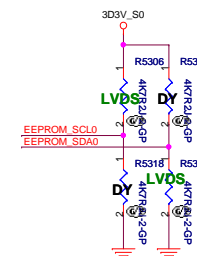
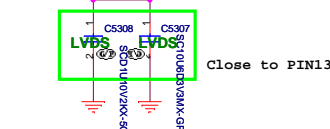
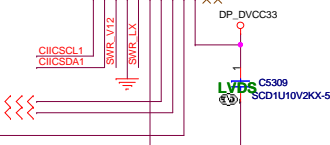
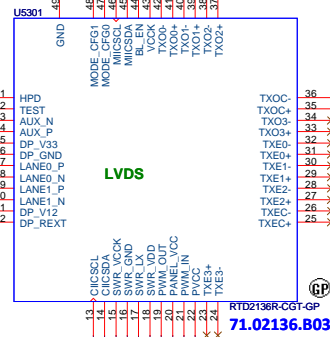
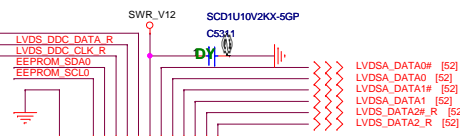
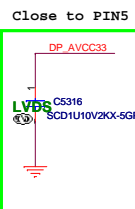
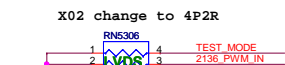
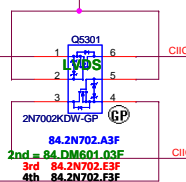
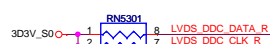
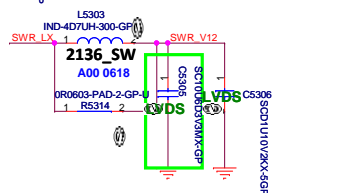
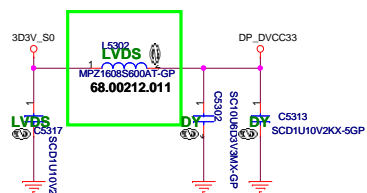
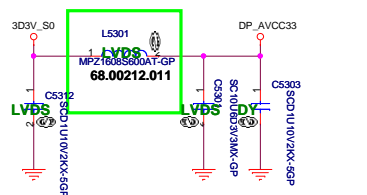
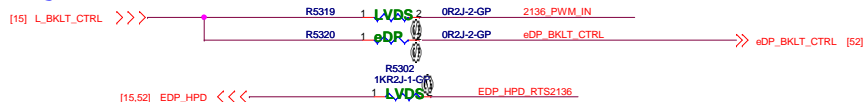
SSID = VIDEO

LVDS & EDP Colay

Layout Note:
Place near U5301



Brightness



Operation Mode Table

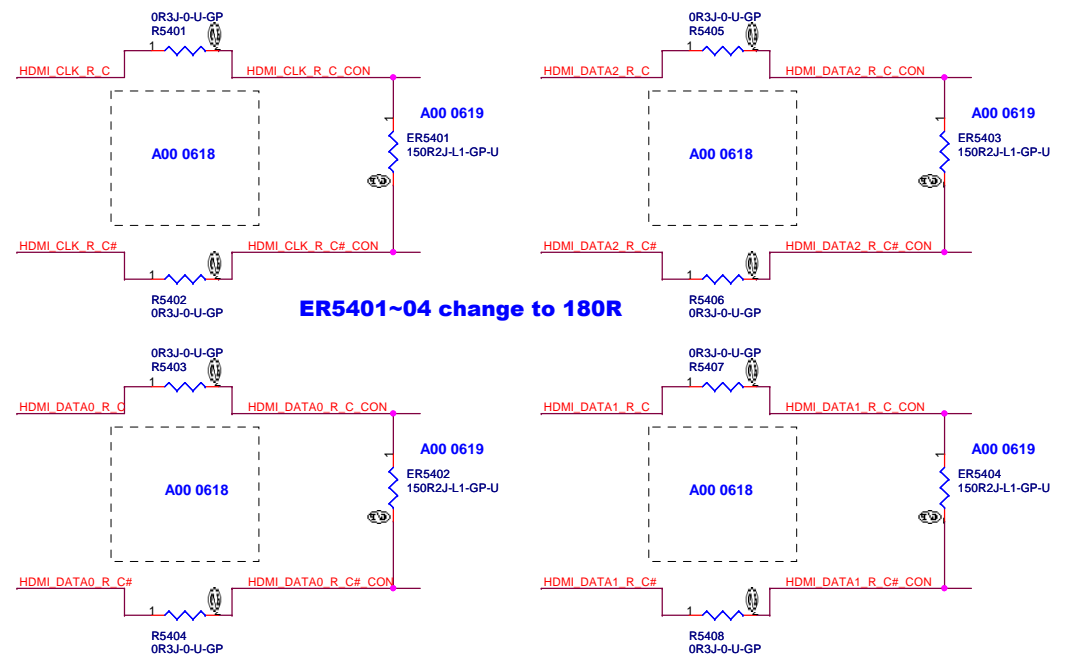
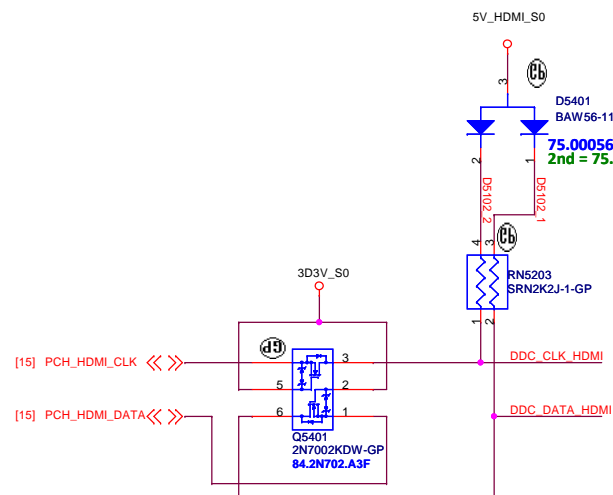
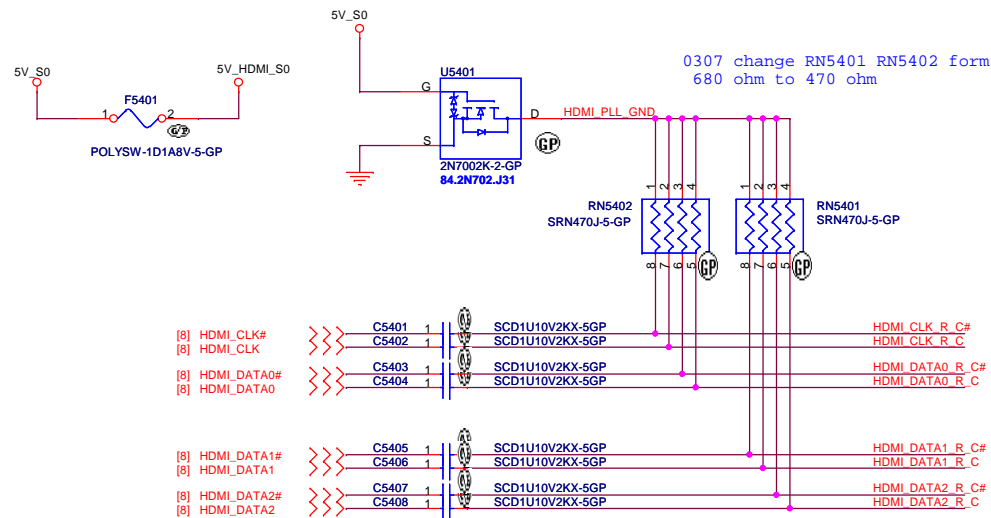
PIN48		PIN47	
		0	1
	0	X	EP Mode
	1	ROM	EEPOM

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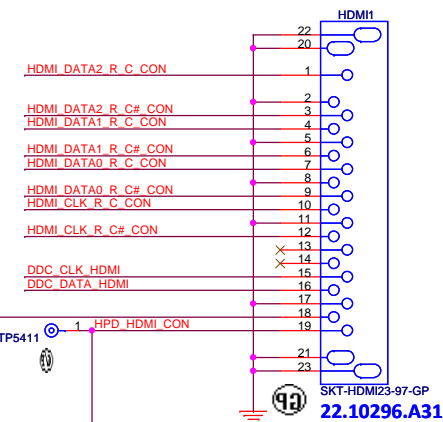
Title				Rev
LVDS Switch				
Size	Document Number			
Custom	Hadley 15"			
Date	Friday, June 21, 2013	Sheet	53 of 101	X02

SSID = VIDEO



ER5401~04 change to 180R

HDMI CONN



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File	HDMI Repeater/Connector		
Size	Document Number	Rev	
A3		X02	
Date	Friday, June 21, 2013	Sheet	54 of 101

(Blanking)

<Core Design>



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Title

Reserved

Size
A3

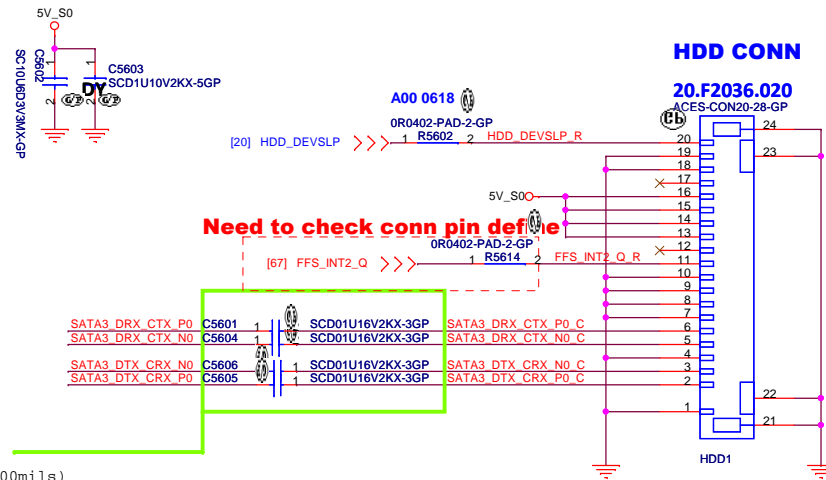
Document Number
Hadley 15"

Date
Friday, June 21, 2013

Rev
X02

Sheet 55 of 101

SSID = SATA



Layout Note:

AC coupling Cap;
place near CONN(<100mils)

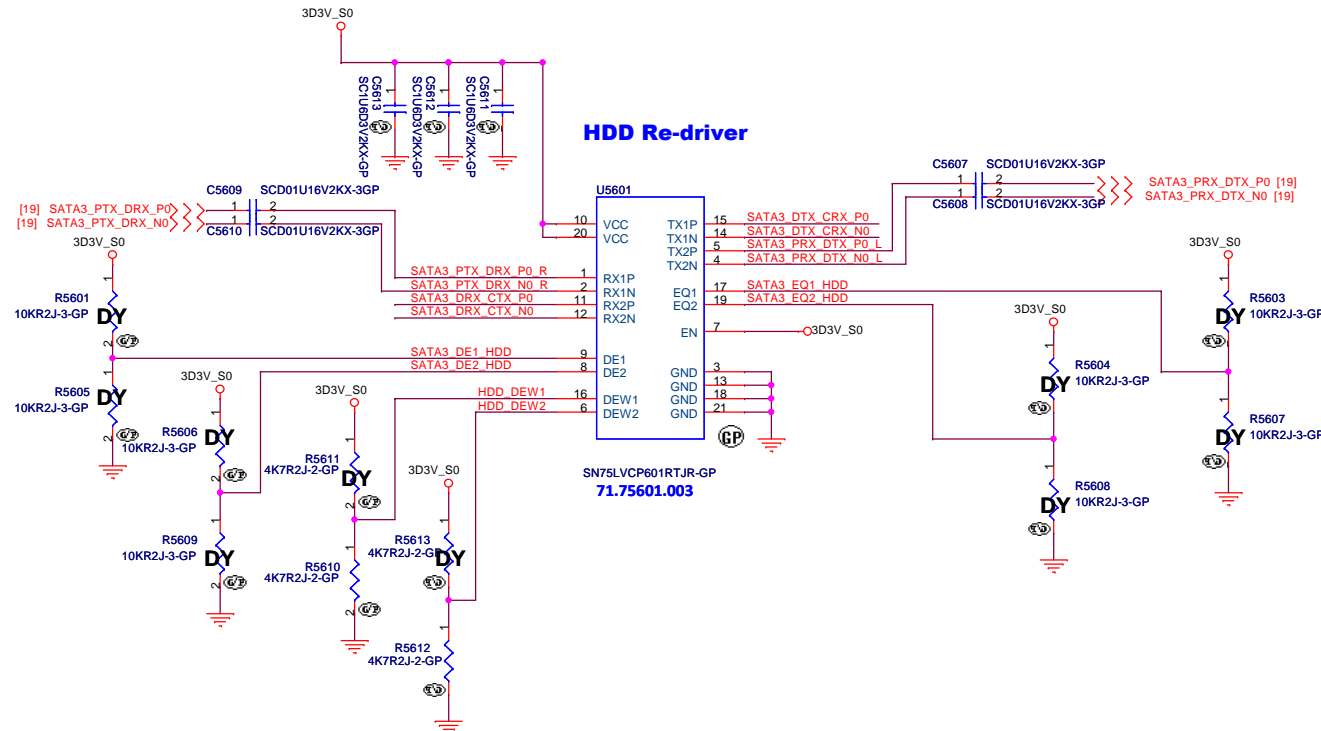


Table 1: Tx/Rx EQ & DE Pulse Width Settings

DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps)
NC (default)	-6
0	0
1	-3

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)
NC (default)	0
0	7
1	14

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

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HDD			Rev
Size A3	Document Number Hadley 15"	X02	
Date	Friday, June 21, 2013	Sheet	56 of 101

(Blanking)

<Core Design>



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Title

Size
A3

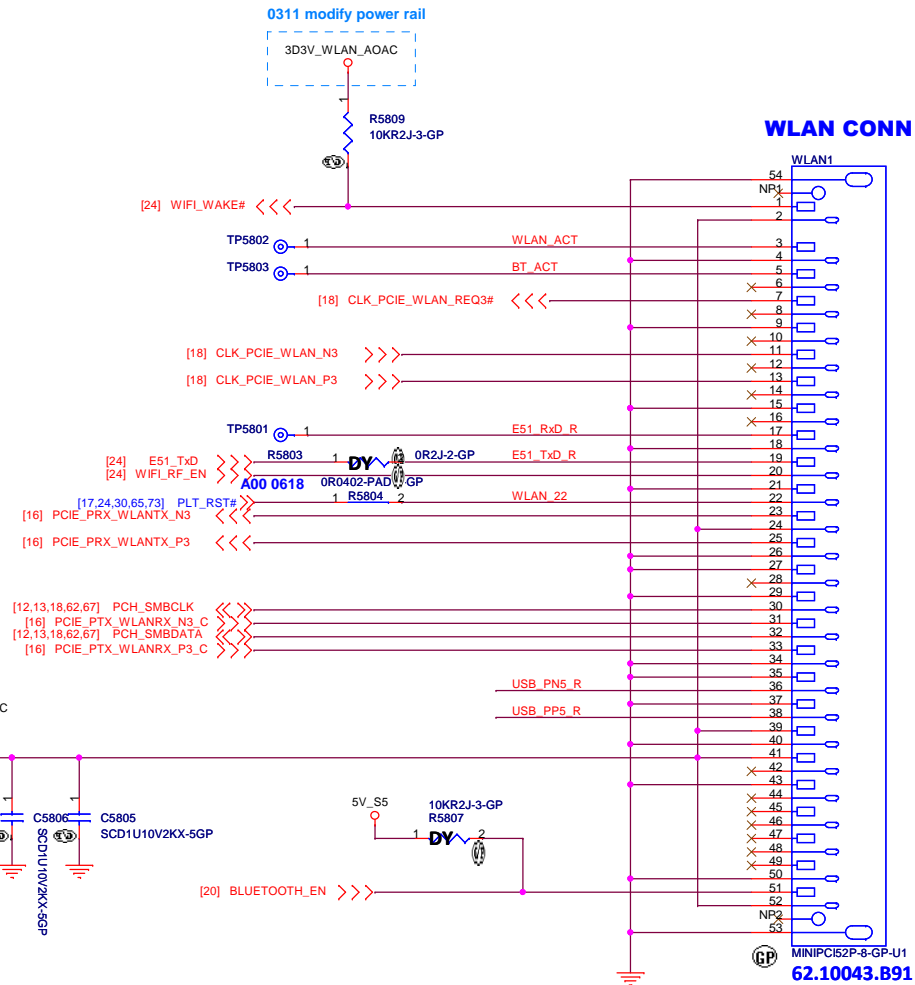
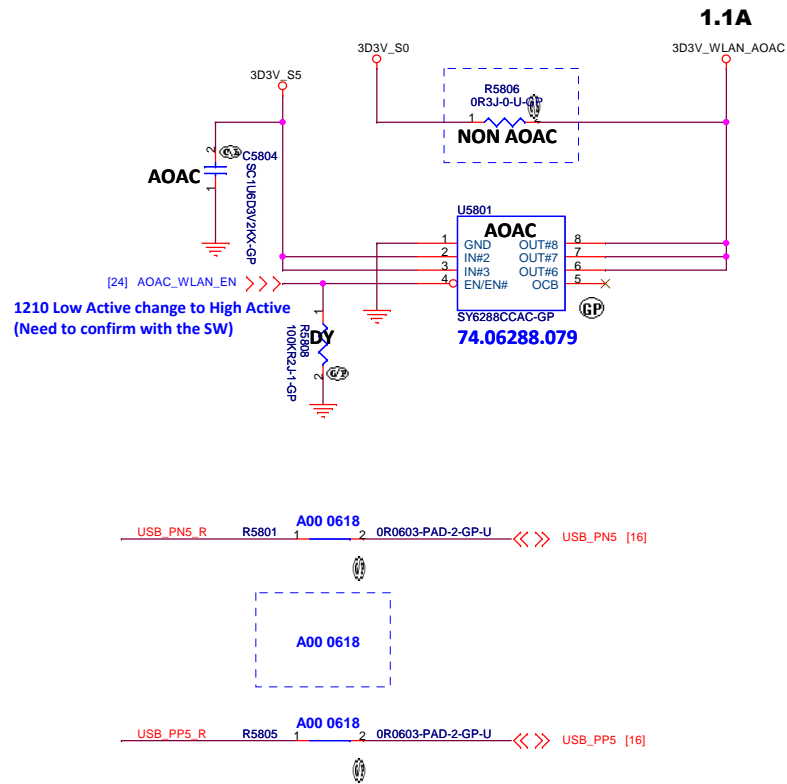
Document Number
Reserved
Hadley 15"

Rev
X02

Date
Friday, June 21, 2013

Sheet
57 of 101

SSID = Wireless



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Title			WLAN/BT	
Size	Document Number	Rev		
A3	Hadley 15"	X02		
Date	Friday, June 21, 2013	Sheet	58	of 101

(Blanking)

<Core Design>



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Title

Reserved

Size
A3

Document Number
Hadley 15"


Date
Friday, June 21, 2013

Rev
X02

Sheet 59 of 101

(Blanking)

<Core Design>



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Title

Reserved

Size
A3

Document Number
Hadley 15"

Rev
X02

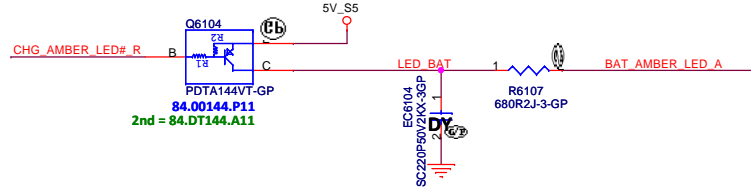
Date
Friday, June 21, 2013

Sheet
60

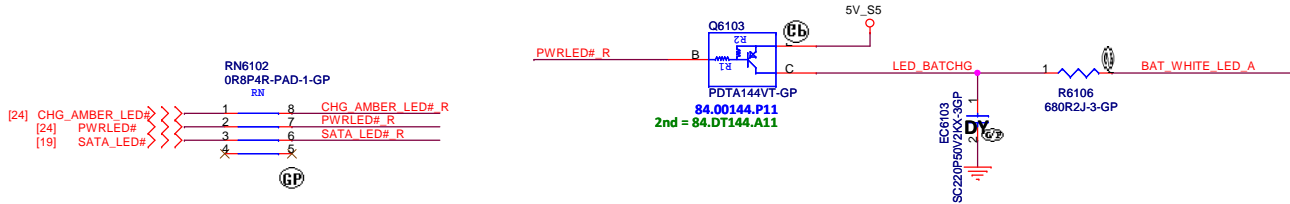
of
101

SSID = User.Interface

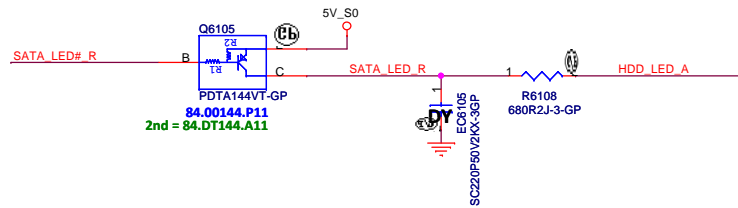
Battery LED1(Amber_LED) LOW acted from KBC GPIO



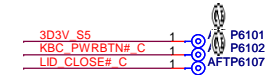
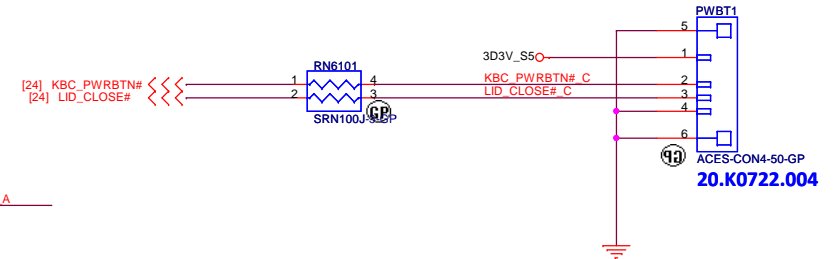
Power & Battery LED2(White_LED) LOW acted from KBC GPIO



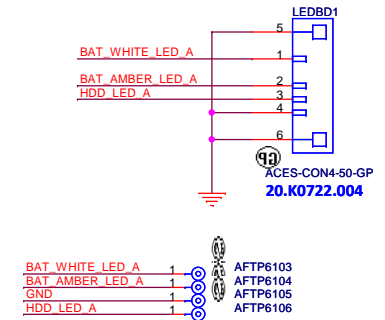
SATA HDD LED



PWRBTN CONN



LED board CONN



<Core Design>

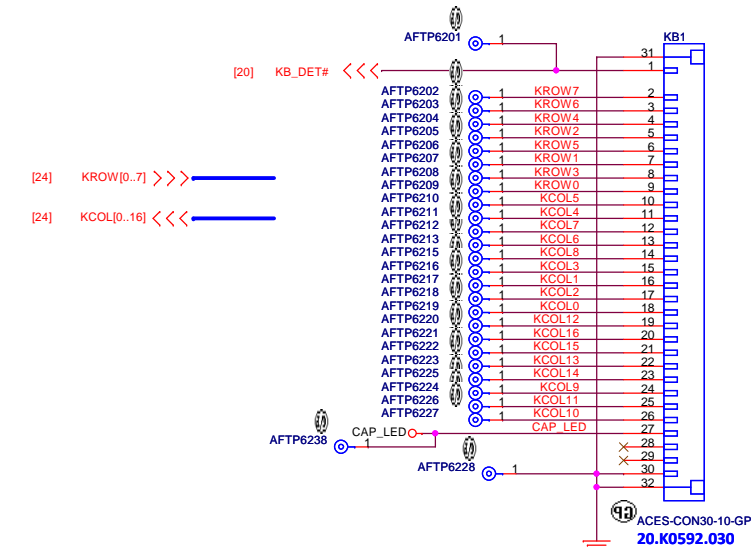


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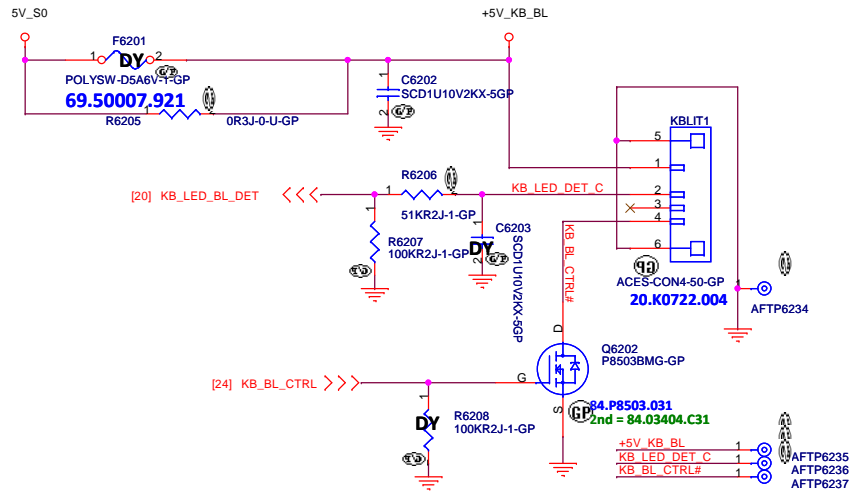
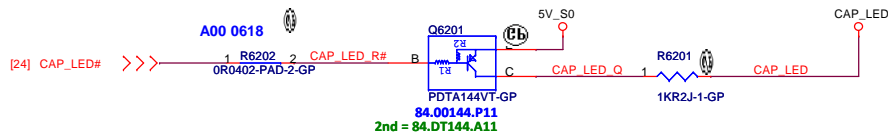
Title		LED Bar/Power Button	
Size	Document Number	Rev	
A3		X02	
Date	Friday, June 21, 2013	Sheet	61 of 101

SSID = KBC

Internal Keyboard Connector

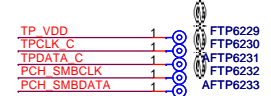
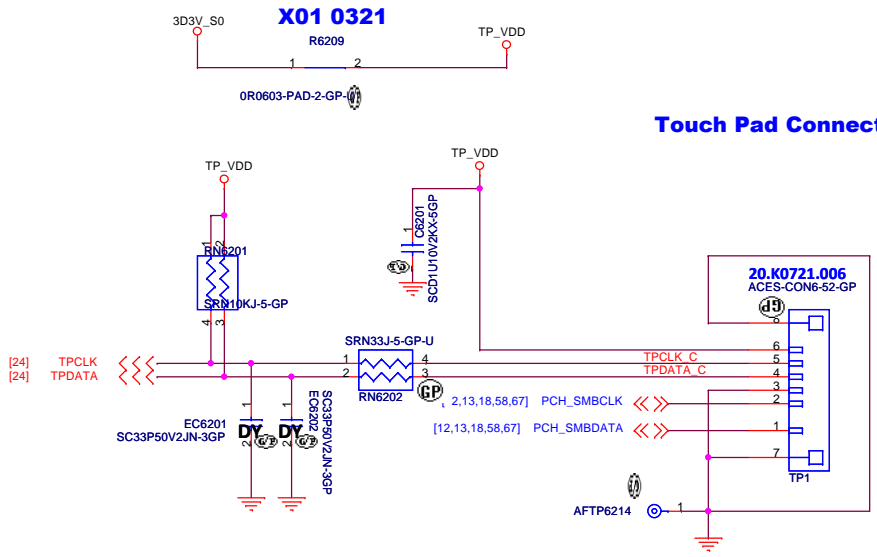


CAP LED Control
LOW acted from KBC GPIO

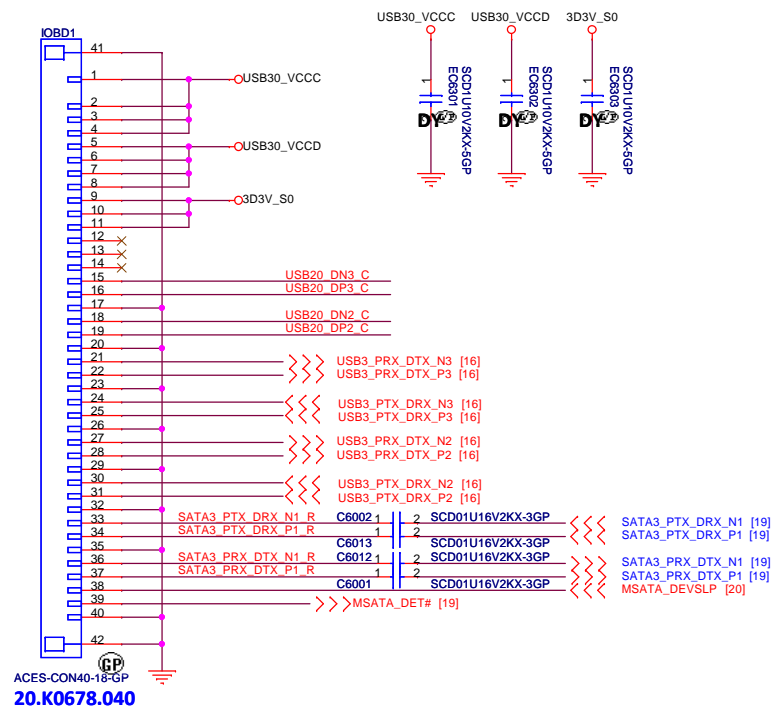


SSID = Touch.Pad

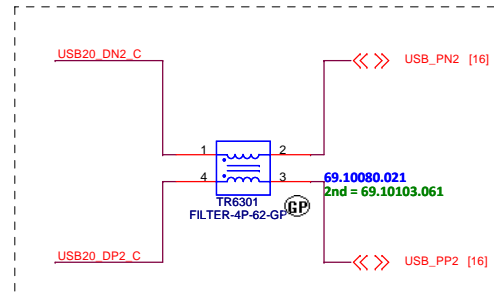
Touch Pad Connector



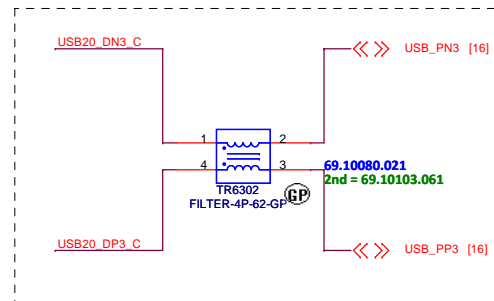
SSID = User.Interface



A00 0618



A00 0618




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Title			
IO Board Connector			
Size	Document Number	Rev	
A3	Hadley 15"	X02	
Date	Friday, June 21, 2013	Sheet	63 of 101

(Blanking)

<Core Design>



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Title

Reserved

Size

A3

Document Number

Hadley 15"

Rev

X02

Date

Friday, June 21, 2013

Sheet

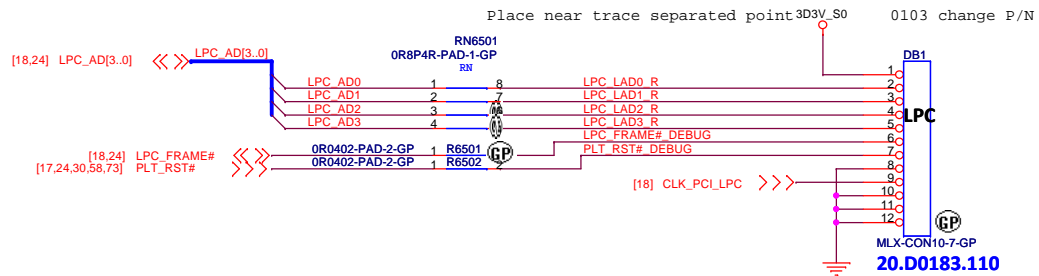
64

of

101

SSID = DEBUG PORT

Debug Connector



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Title

Dubug connector

Size

Document Number

Hadley 15"

Rev

X02


Date

Friday, June 21, 2013

Sheet 65 of 101

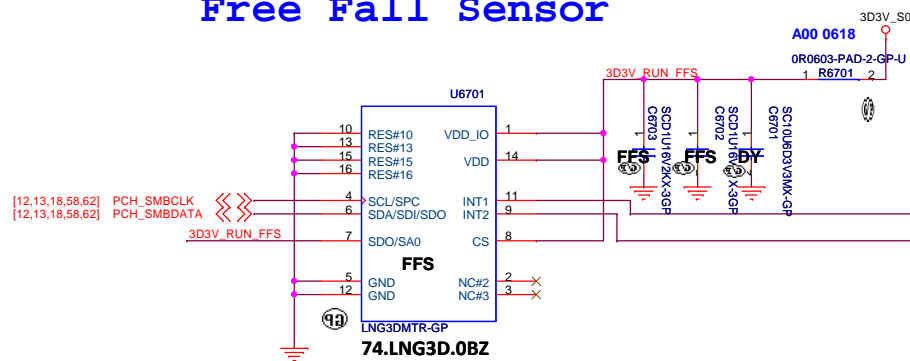
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Title			
Reserved			
Size A4	Document Number Hadley 15"		Rev X02
Date: Friday, June 21, 2013		Sheet 66	of 101

```
SSID = User.Interface
```

Free Fall Sensor

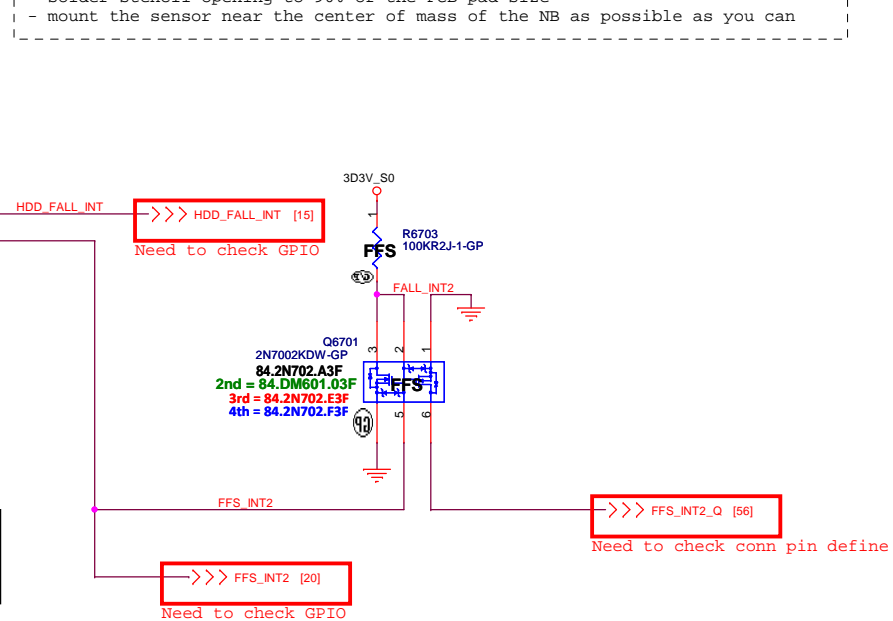


Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



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Size	A3
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Document Number **Ha**

Rev


X02

Date Friday, June 21, 2013

Sheet 67 of 101

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Title

Reserved

Size A3	Document Number Hadley 15"	Rev X02
Date Friday, June 21, 2013	Sheet 68	of 101

(Blanking)

<Core Design>



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Title

Reserved

Size
A3

Document Number
Hadley 15"

Rev
X02


Date
Friday, June 21, 2013

Sheet
69

of
101

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.


Title

Reserved

Size A3	Document Number Hadley 15"	Rev X02
Date Friday, June 21, 2013	Sheet 70	of 101

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
Hadley 15"

Rev
X02


Date
Friday, June 21, 2013

Sheet
71

of
101

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
Hadley 15"

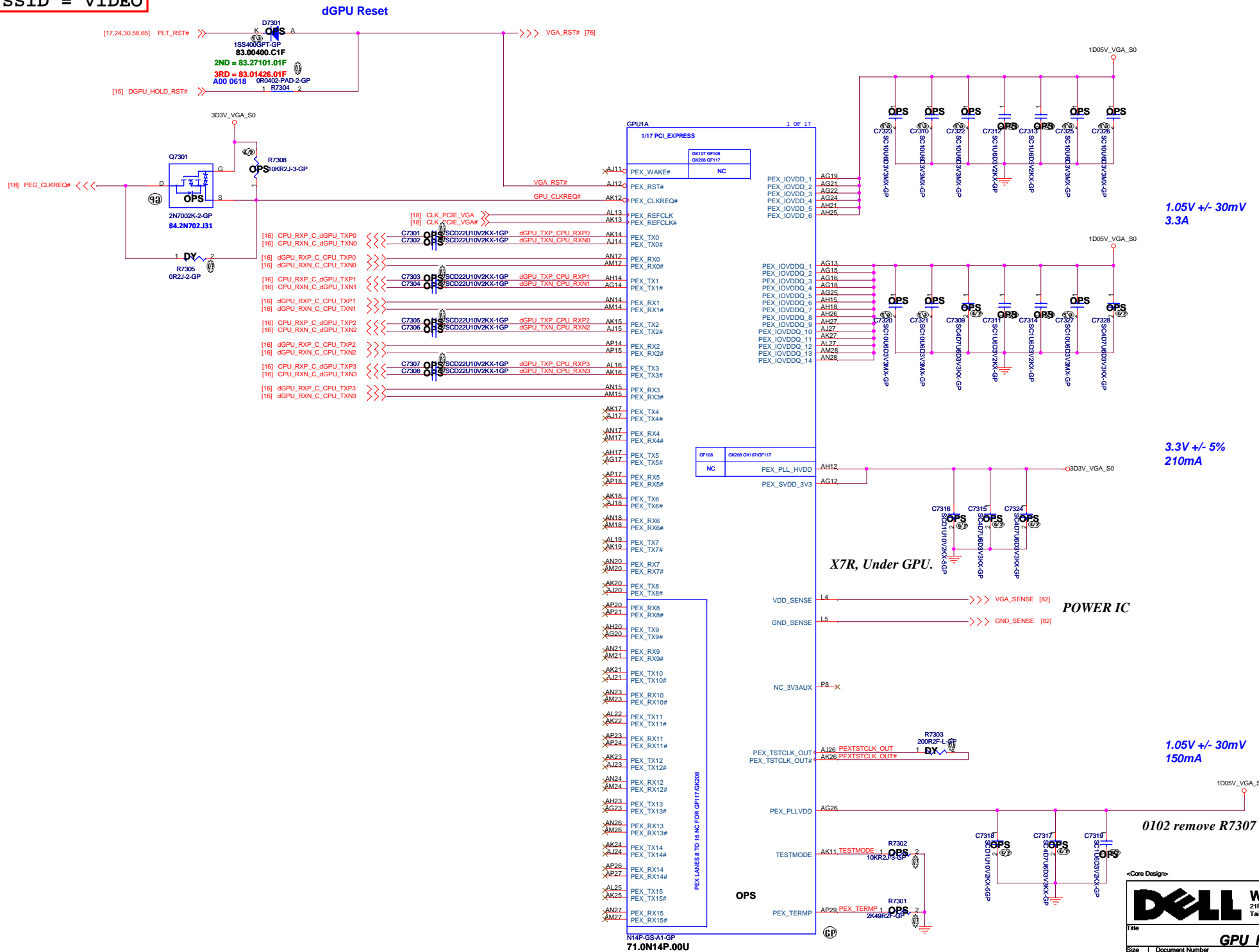
Rev
X02

Date
Friday, June 21, 2013

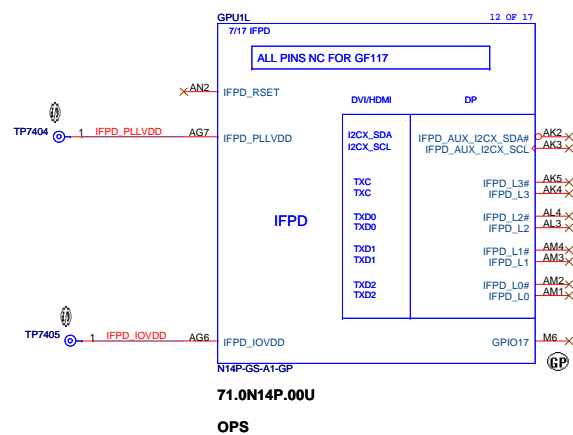
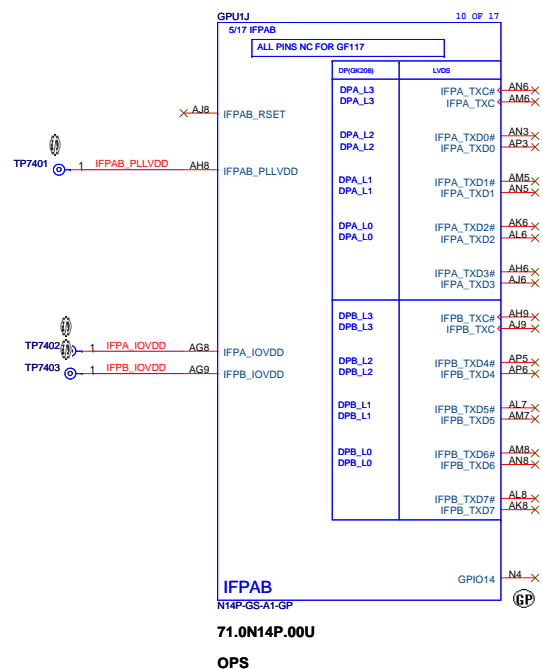
Sheet
72

of
101

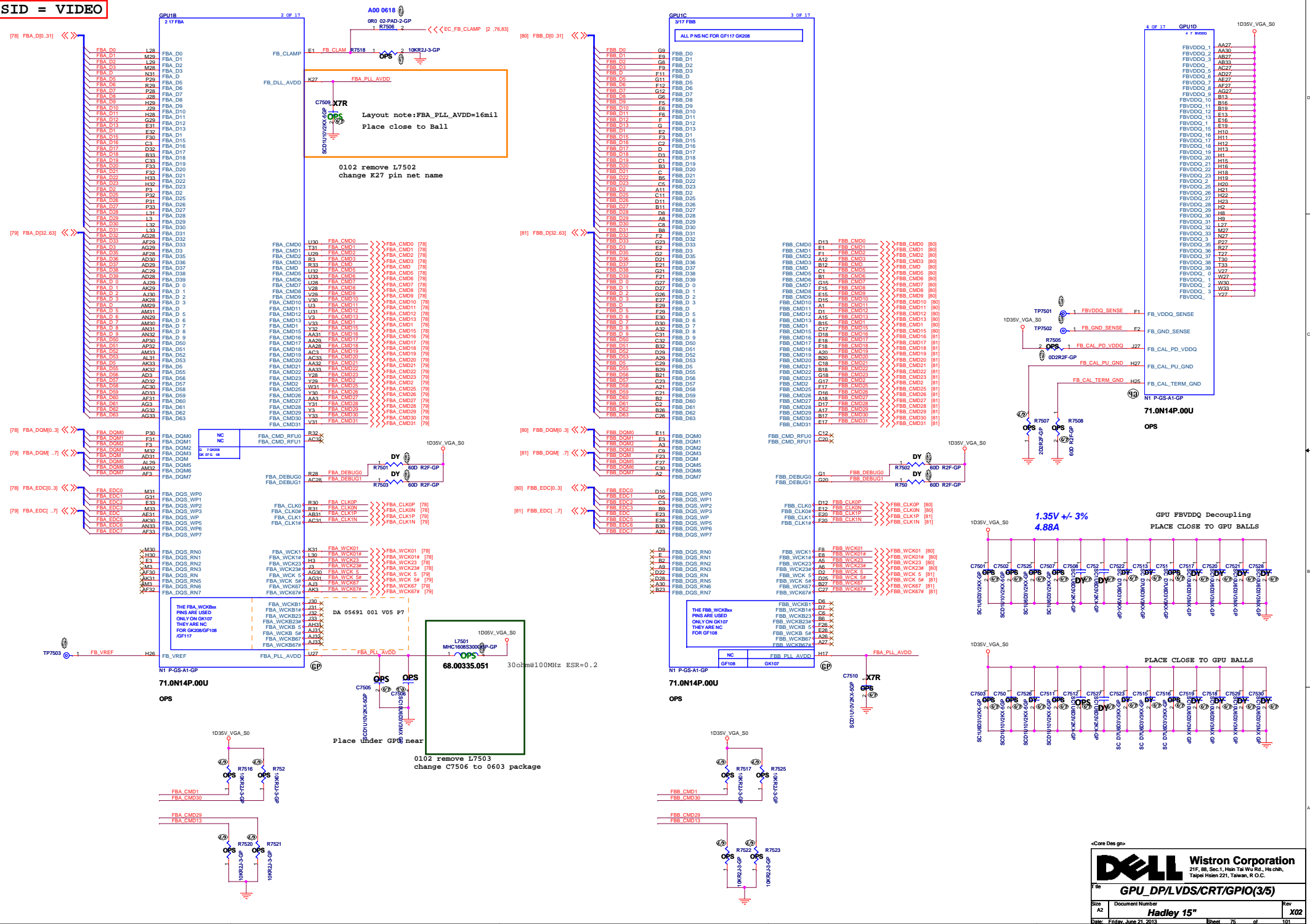
SSID = VIDEO



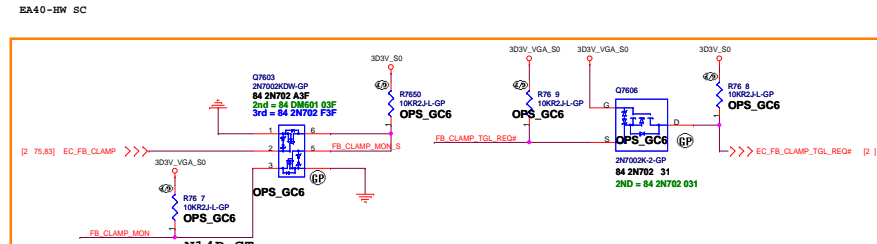
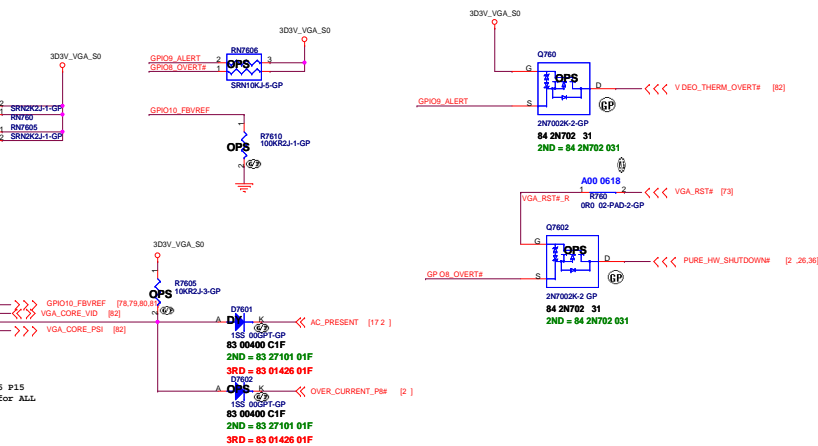
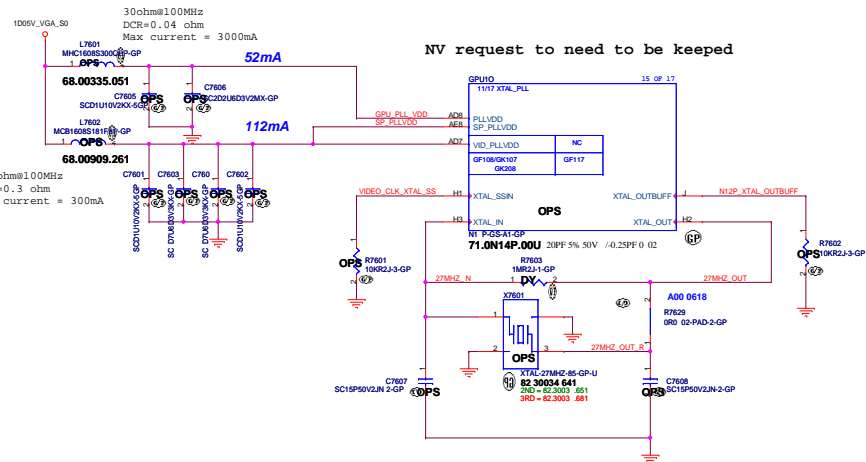
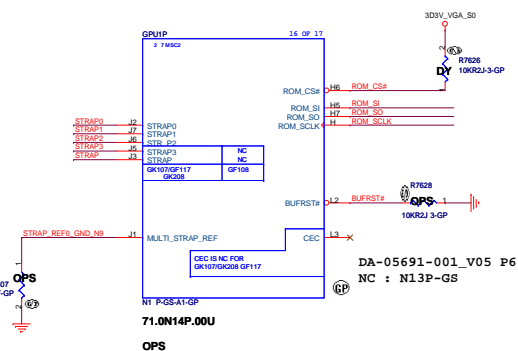
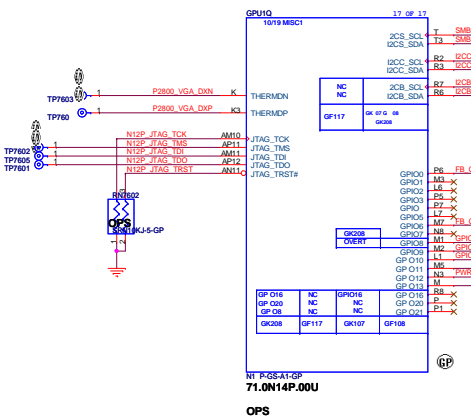
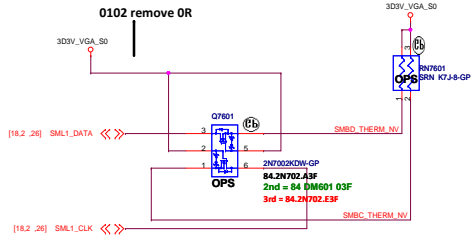
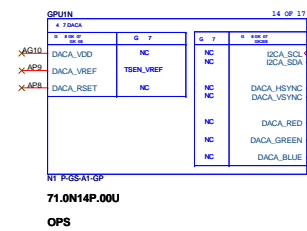
SSID = VIDEO



SSID = VIDEO



SSID = VIDEO

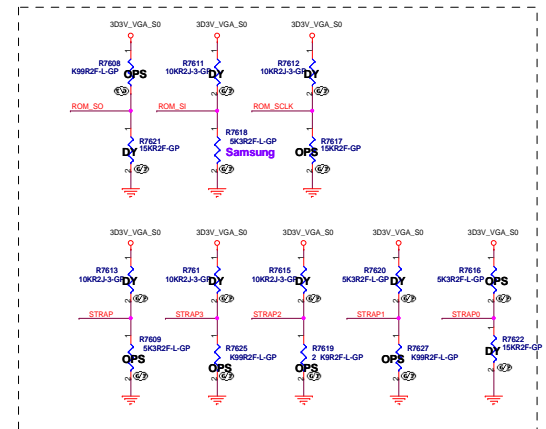


Resistor Values	Pull-up to VDD33	Pull-down to GN
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

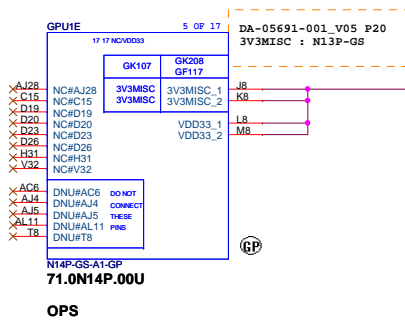
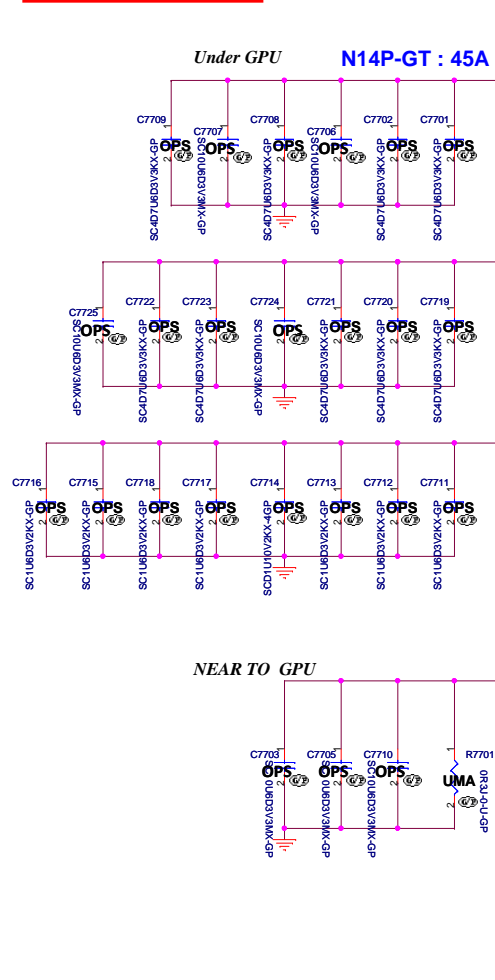
GPU Product Name	N14P-GT
NV-Internal Chip Part# (used on labels of packaging bag/box materials)	GK107-750
Device ID	0x0FE4
Memory interface	GDDR5
Package	GB4-128

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x6	1.35V/ 1.35V	H5GQ24H4FR-T2C	2000	N/A	Production candidate
	Samsung	0x7	1.35V/ 1.35V	K4G23025FD-FC04	2000	1219	Post-production candidate

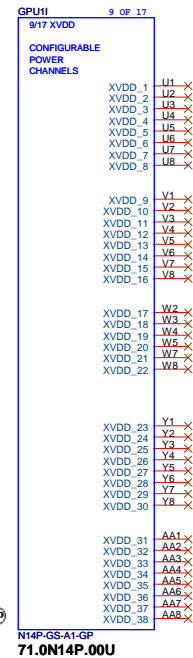
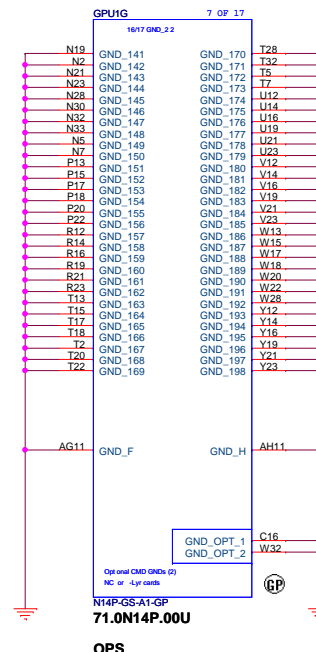
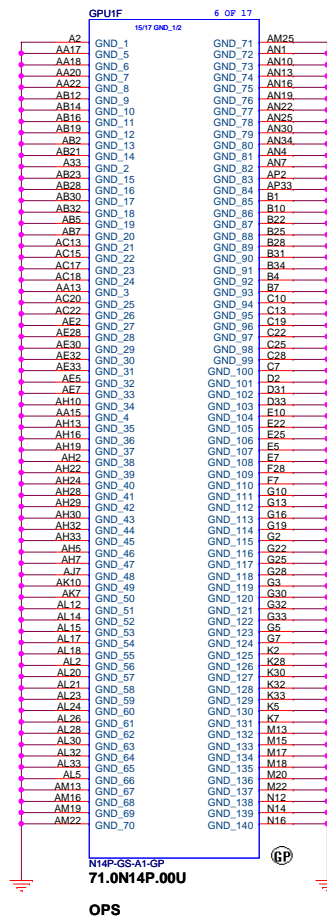
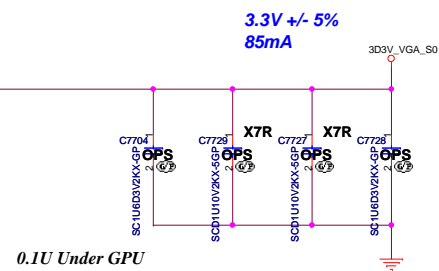
Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	0 PCI_DEVID[4]	0 SUB_VENDOR	1 PCI_DEVID[5]	0 PEX_PLL_EN_TERM
ROM_S#	0 RAM_CFG[3]	1 RAM_CFG[2]	1 RAM_CFG[1]	1 RAM_CFG[0]
ROM_SD	1 FB[1]	0 FB[0]	0 SMB_ALT_ADDR	0 VGA_DEVICE
STRAP0	1 USER[3]	0 USER[2]	1 USER[1]	1 USER[0]
STRAP1	0 3GIO_PADCFG[3]	0 3GIO_PADCFG[2]	0 3GIO_PADCFG[1]	0 3GIO_PADCFG[0]
STRAP2	0 PCI_DEVID[3]	1 PCI_DEVID[2]	0 PCI_DEVID[1]	0 PCI_DEVID[0]
STRAP3	0 S0R1_EXPOSED	0 S0R2_EXPOSED	0 S0R1_EXPOSED	0 S0R0_EXPOSED
STRAP4	0 RESERVED	0 PCIE_SPEED_CHAN_GEN[5]	1 PCIE_MAX_SPEED	0 DP_PLL_VDD033V



SSID = VIDEO

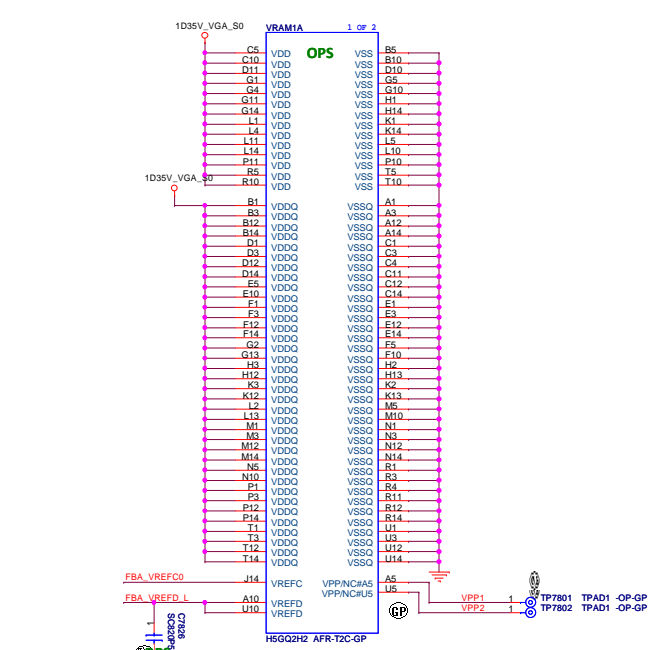


0.1U Under GPU
4.7U NEAR TO GPU
1U NEAR TO GPU

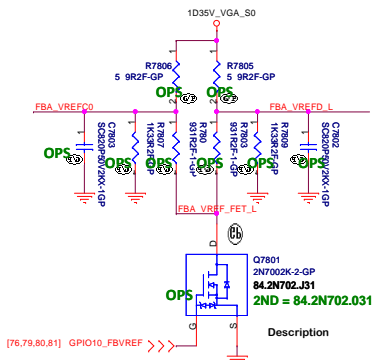


Title				GPU POWER(4/5)			
Size	Document Number					Rev	
Cust	m	Hadley 15"				X02	
Date	Friday June 21 2013	Sheet	77	of	101		

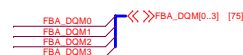
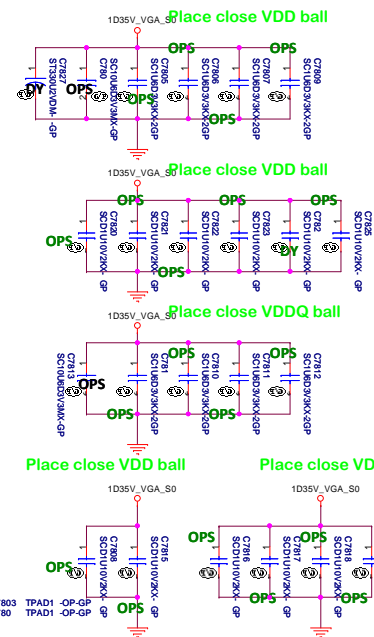
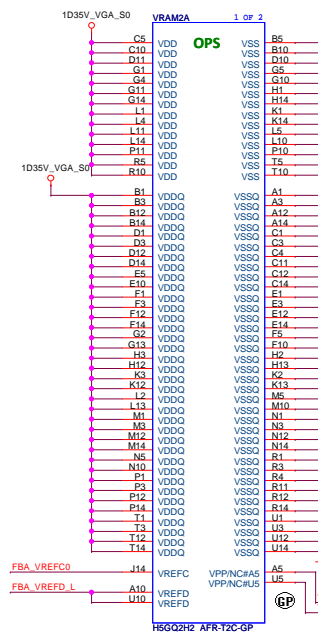
SSID = VIDEO



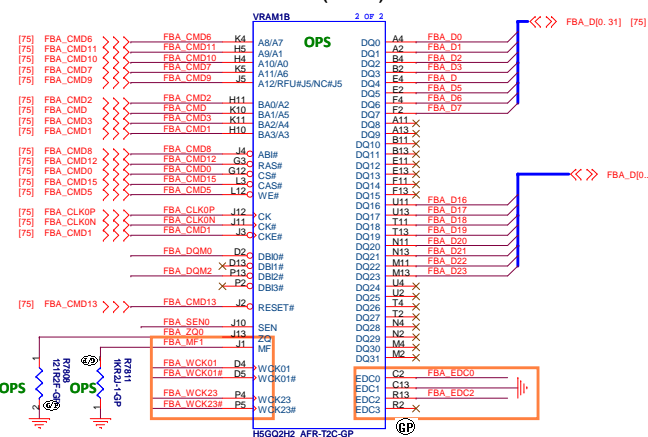
Frame Buffer Patition A-Lower Half



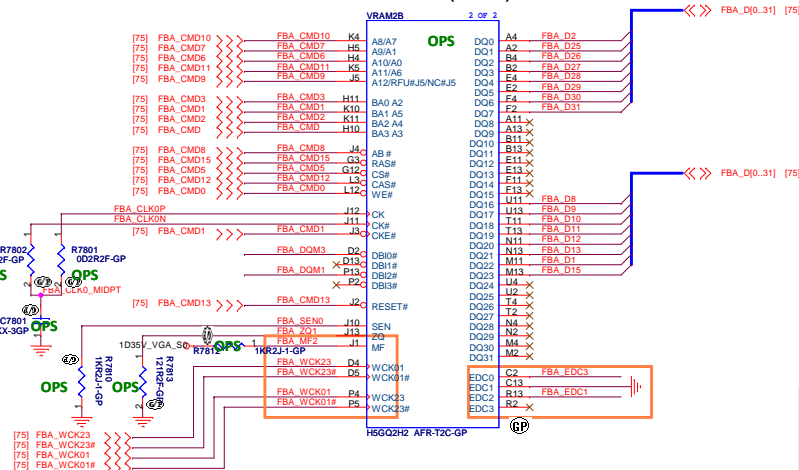
Type	FBVREF%	Voltage	GPU_GPIO1
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



Normal(MF=0)



Mirrored(MF=1)



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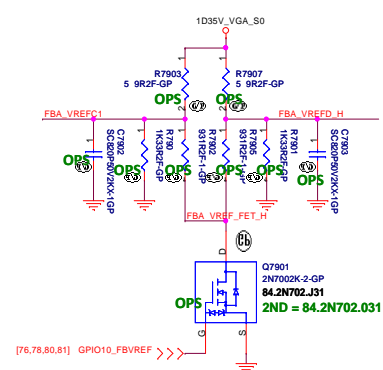


Title		GPU-VRAM1,2 (1/4)		Rev	
Size	Document Number	Hadley 15"		X02	
Customer	Date: Friday, June 21, 2013		Sheet 78 of 101		

WWW.AliSaler.Com

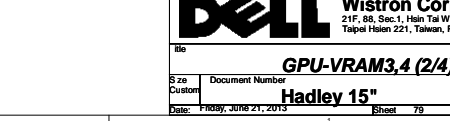
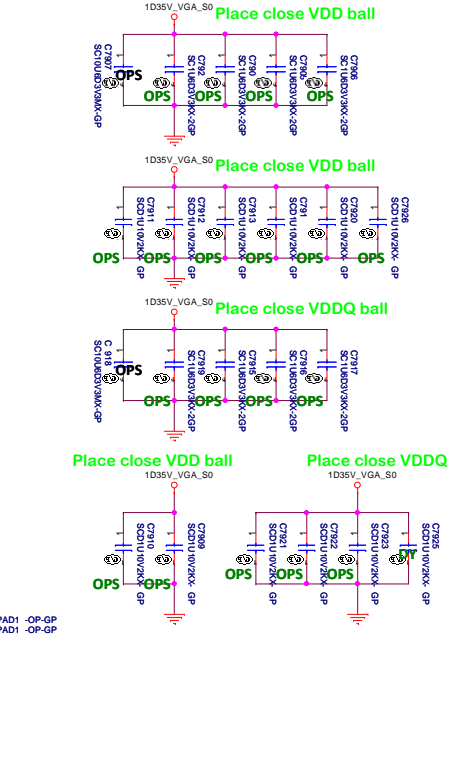
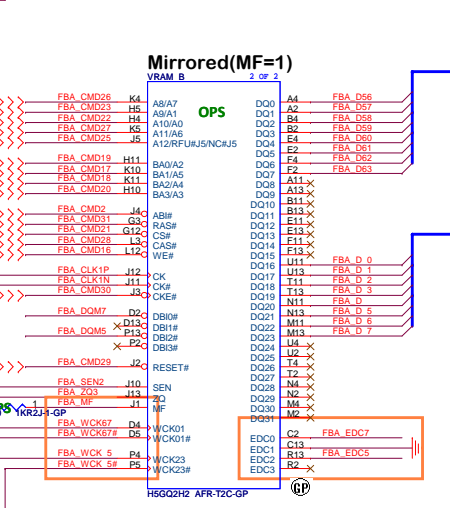
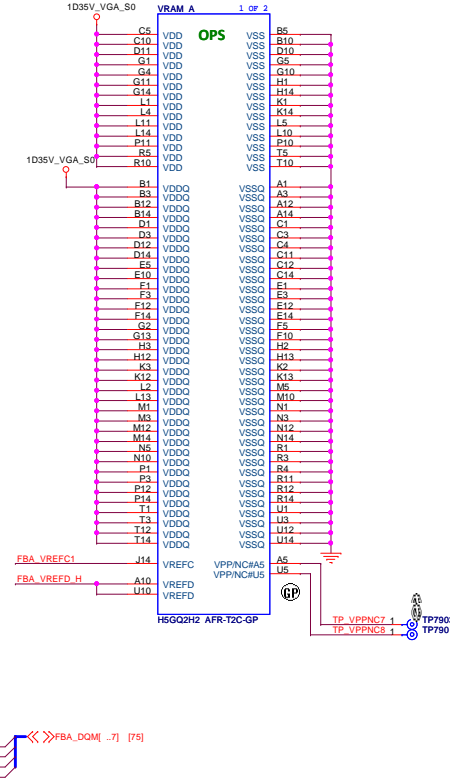
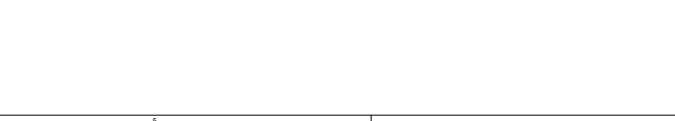
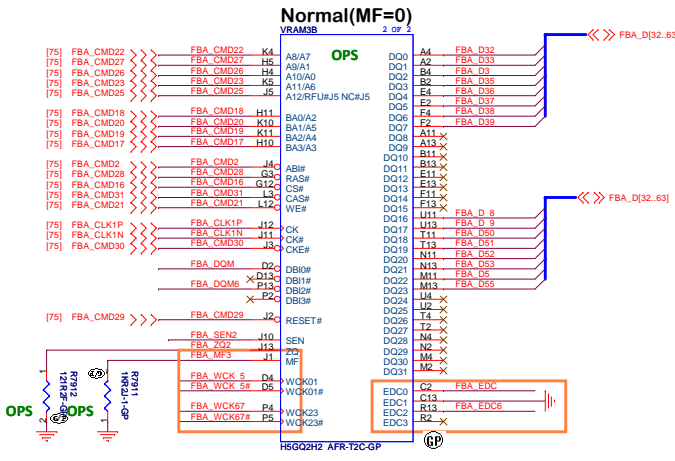
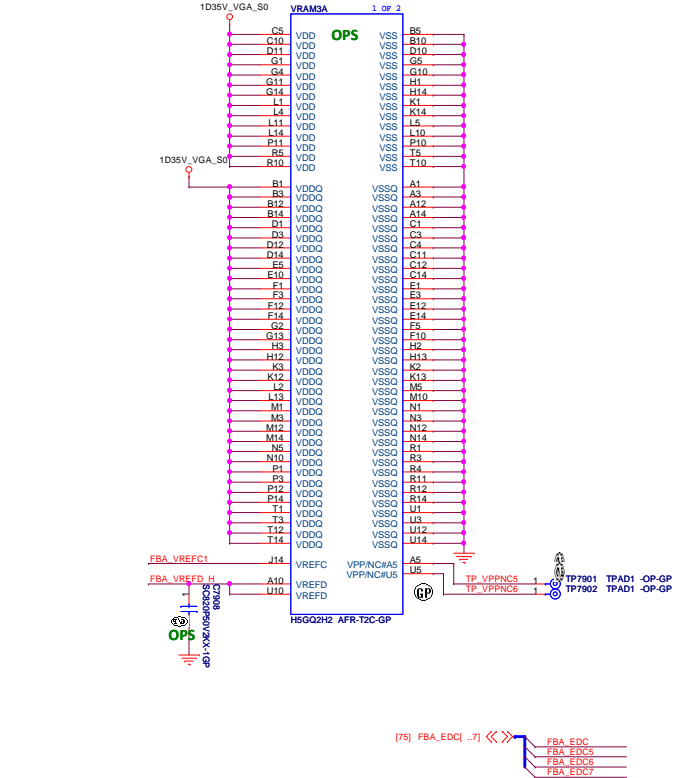
SSID = VIDEO

Frame Buffer Partition A-Upper Half

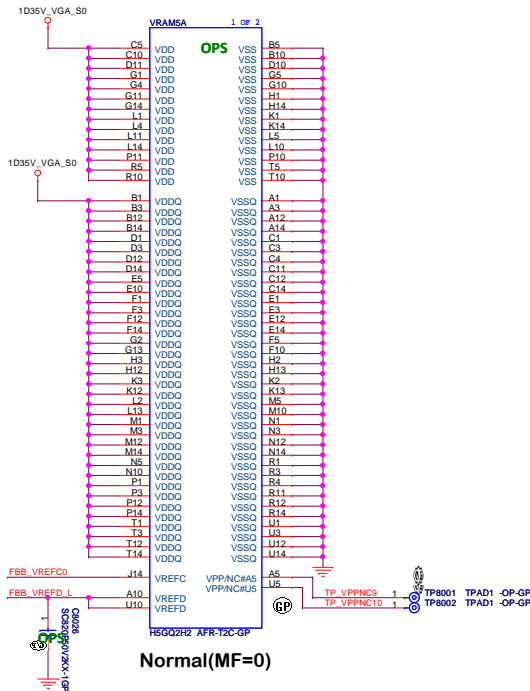


FBVREF Termination

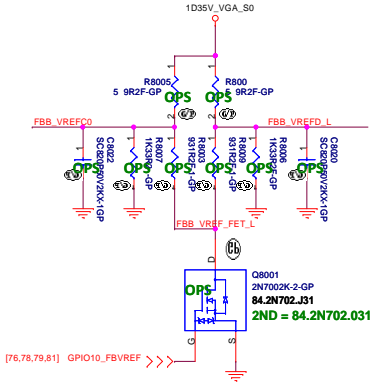
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



SSID = VIDEO

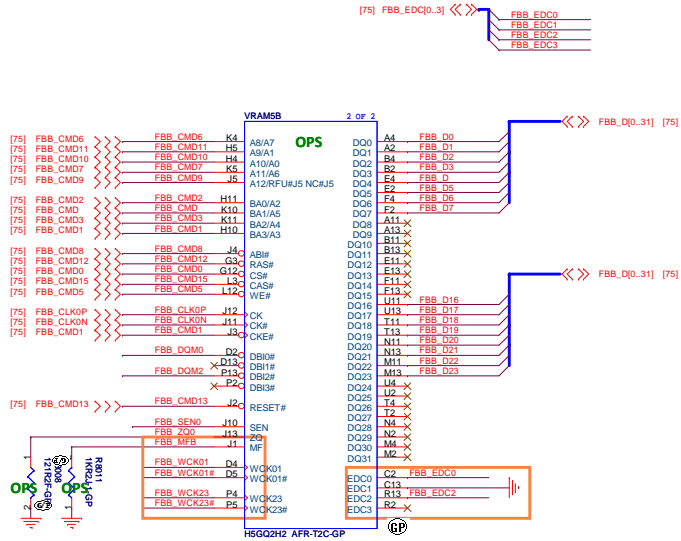
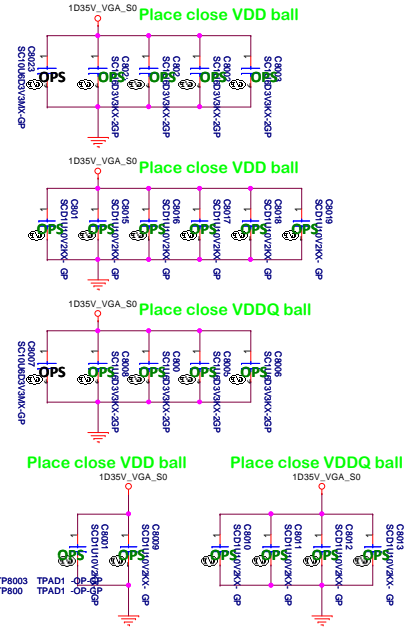
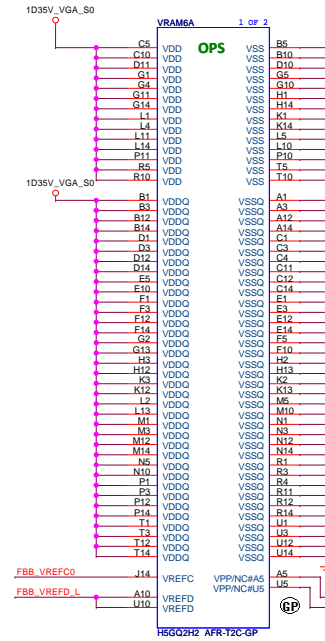


Frame Buffer Partition B-Lower Half

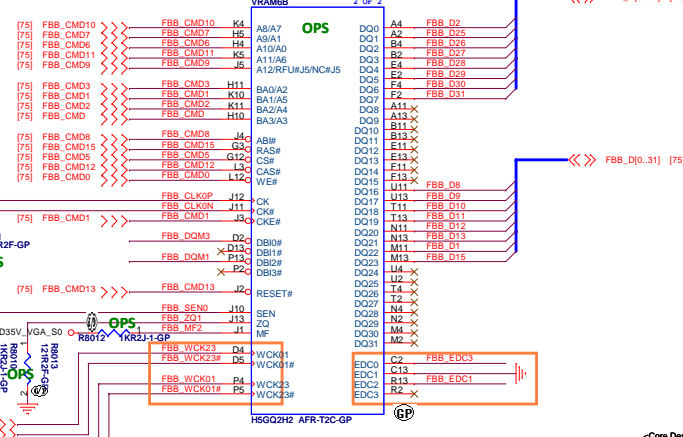


FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



Mirrored(MF=1)

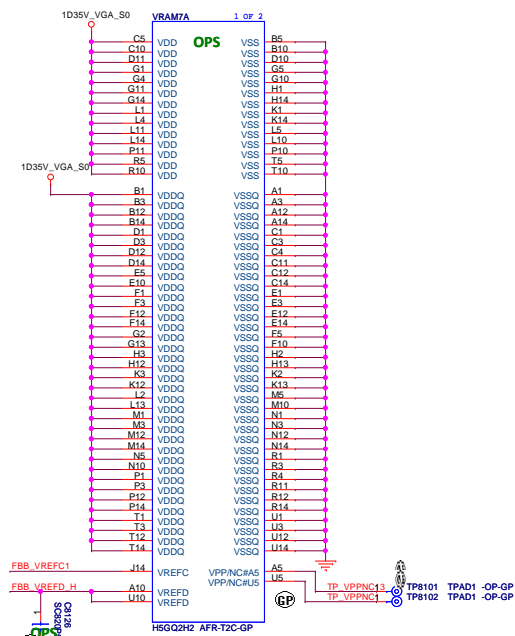


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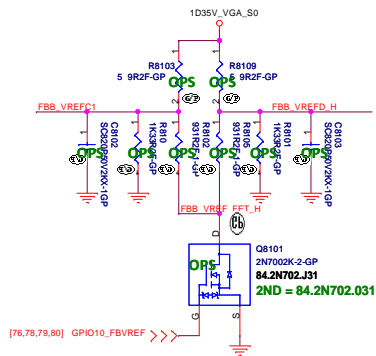


GPU-VRAM5,6 (3/4)		
Rev	Document Number	X02
Hadley 15"		
Date: Friday, June 21, 2013	Sheet 80 of 101	

SSID = VIDEO

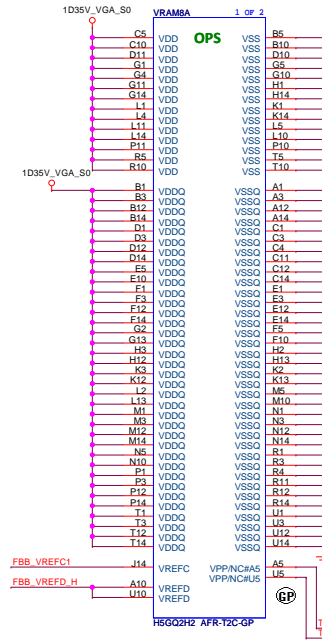


Normal(MF=0)

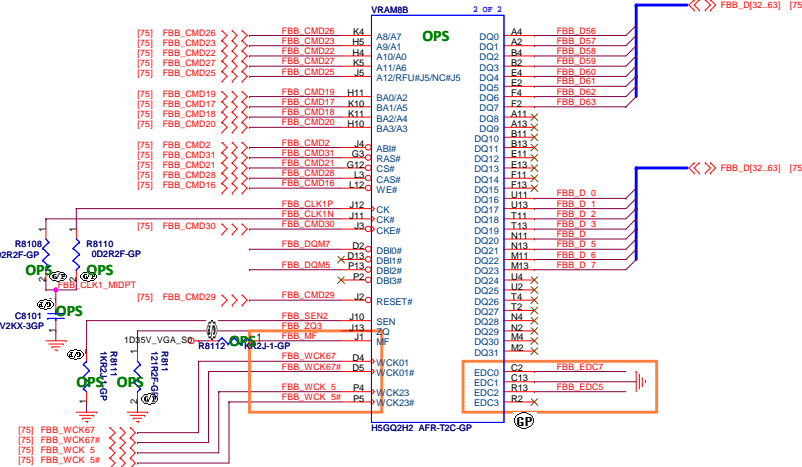
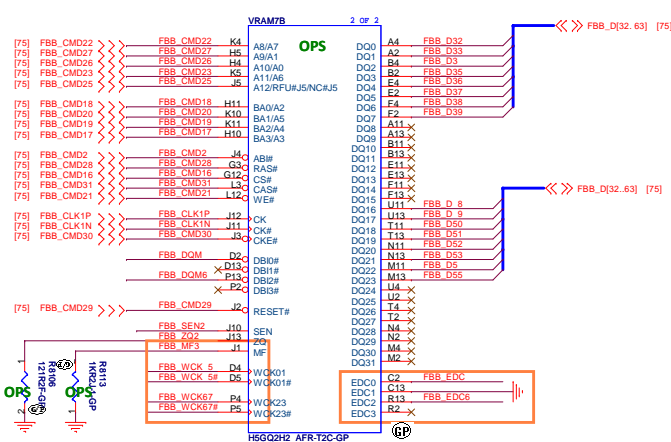
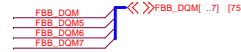
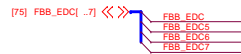
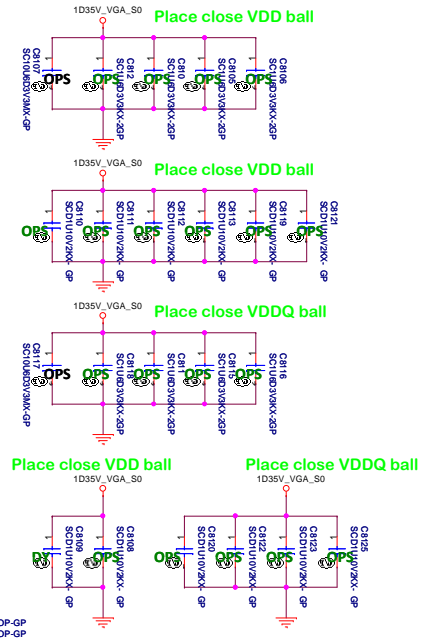


FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



Mirrored(MF=1)

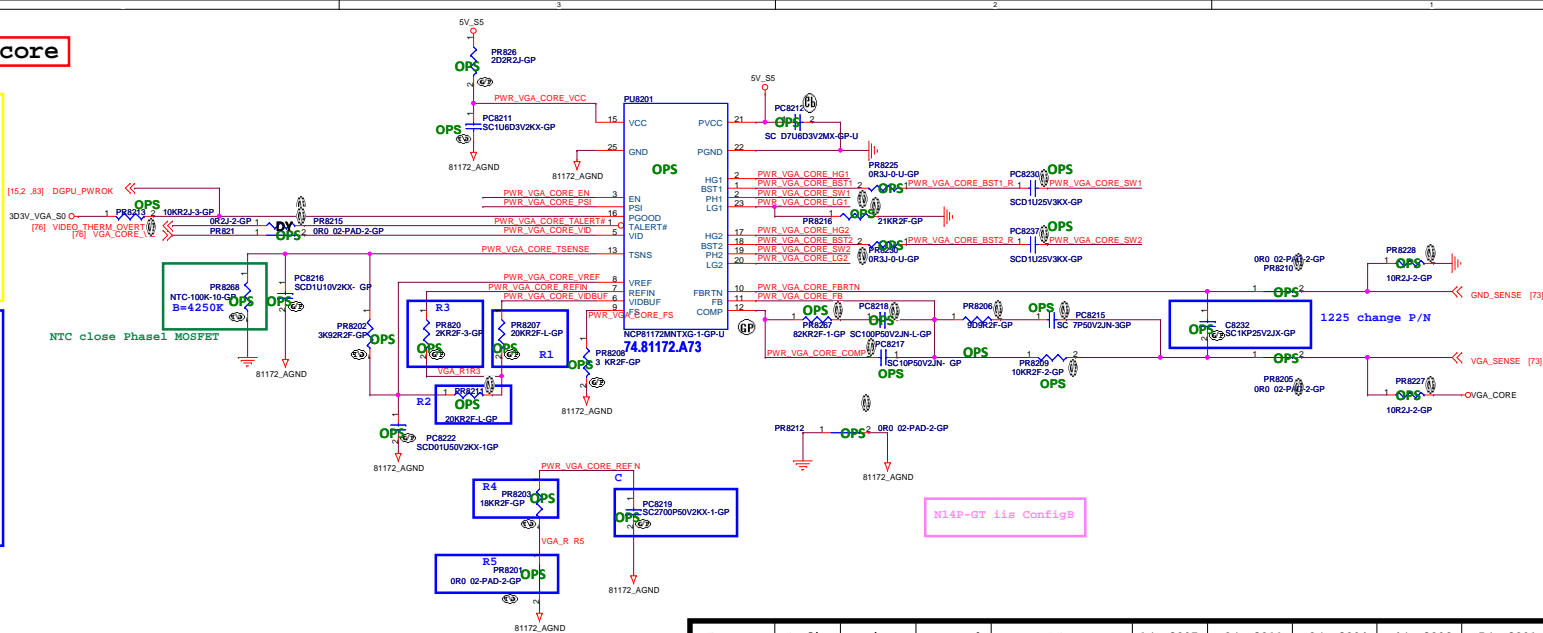
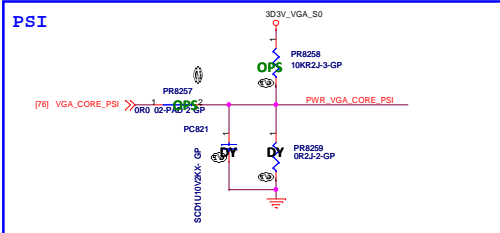
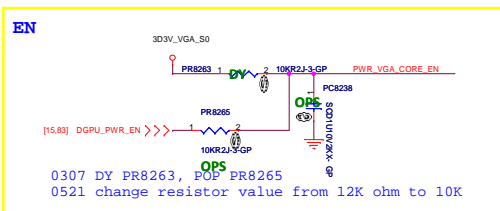


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file			
GPU-VRAM7,8 (4/4)			
Size Custom	Document Number		Rev
	Hadley 15"		X02
Date:	Friday, June 21, 2013		Sheet 51 of 101

SSID = PWR.Plane.Regulator vga core

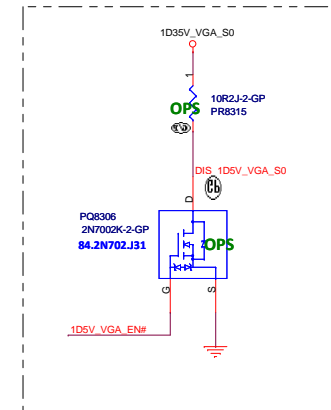
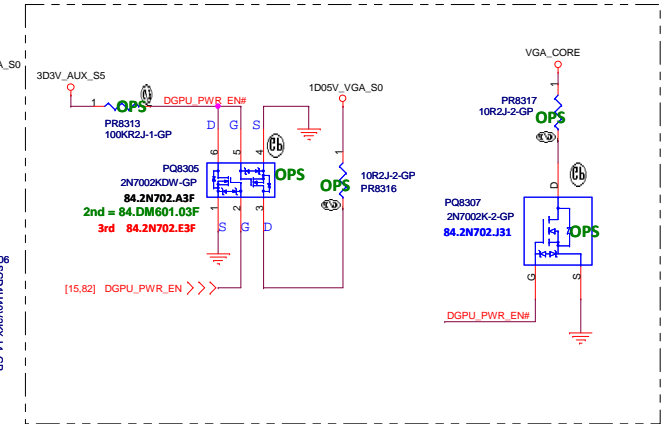


VGA type	Config	Design Current	EDP-peak	OCF	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14P-LP	B	25A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GE	B	27A	40A	44A<OCP<52A	20K	20K	2K	18K	0	2.7nF
N14P-GS	B	38A	60A	66A<OCP<78A	20K	20K	2K	18K	0	2.7nF
N14P-TS	B	45A	75A	82.5A<OCP<97.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV	B	24A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV2	B	32A	55A	60.5A<OCP<71.5A	20K	20K	2K	18K	0	2.7nF
N14M-GS	B	26A	45A	49.5A<OCP<58.5A	20K	20K	2K	18K	0	2.7nF
N14M-LP	B	22A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14M-GL	C	24.33A	35.42A	38.96A<OCP<46.04A	39K	30K	3K	24K	3K	1.8nF
N14M-GE	C	35A	40.89A	44.98A<OCP<53.16A	39K	30K	3K	24K	3K	1.8nF
N14E-GTX	A	95A	125A	137.5A<OCP<162.5A	39K	39K	1.5K	30K	1.5K	1.5nF
N14E-GS	B	65.16A	87.87A	96.66A<OCP<114.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE-B	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GL	B	46.35A	71.83A	79.01A<OCP<93.98A	20K	20K	2K	18K	0	2.7nF

Table 1. PWM-VID Spec and Component Values


PWM-VID Spec	Config A	Config B	Config C
Vmin	V	0.6	0.65
Vmax	V	1.2	1.15
Vboot	V	0.875	0.9
Voltage Step Vstep	mV	6.25	6.25
Number of Voltage Levels N	level	96	96
PWM Frequency F _{PWM}	MHz	1.125	1.125
PWM Minimum Pulse Width T _{DMH}	ns	9.26	9.26
VID Transient Time T	us	<100	<100
Component Value			
R1 (1%)	KΩ	39	39
R2 (1%)	KΩ	39	30
R3 (1%)	KΩ	1.5	2
R4 (1%)	KΩ	30	18
R5 (1%)	KΩ	1.5	0
C	nF	1.5	2.7

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Title

Size
A3

Document Number
Reserved
Hadley 15"

Rev
X02


Date
Friday, June 21, 2013

Sheet
84

of
101

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<Core Design>



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Size

A3

Document Number

Hadley 15"

Date

Friday, June 21, 2013

Rev

X02

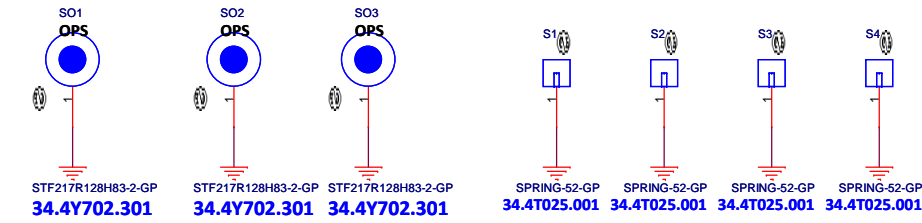
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85

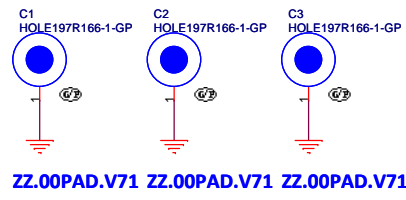
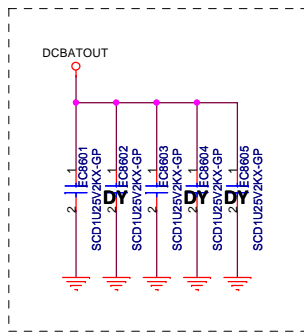
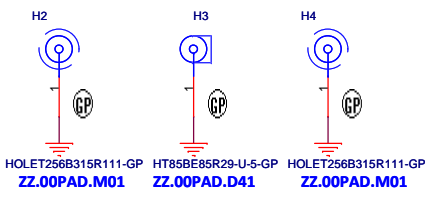
 of

101

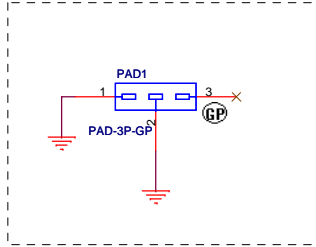
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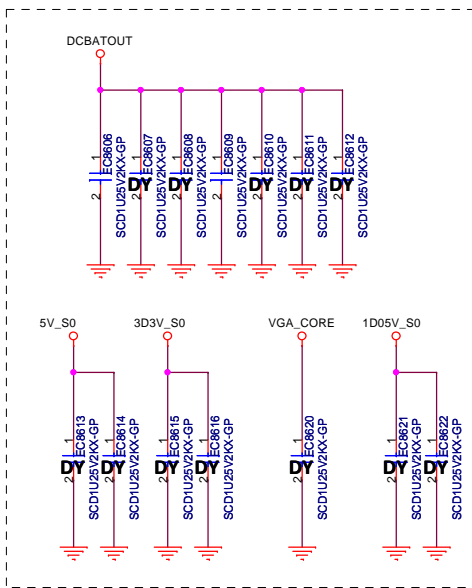
0116 Add RF CAP



0528 Add NPTH hole



0117 Add EMC CAP



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UNUSED PARTS/EMI Capacitors

Size A3 Document Number
Hadley 15"

Date Friday, June 21, 2013 Sheet 86 of 101 Rev X02

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Title

Reserved

Size
A3

Document Number
Hadley 15"

Rev
X02


Date
Friday, June 21, 2013

Sheet
87

of
101

(Blanking)

<Core Design>



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Title

Size
A3

Document Number
Hadley 15"


Date
Friday, June 21, 2013

Rev
X02

Sheet 88 of 101

(Blanking)

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Title

Reserved

Size

A3

Document Number

Hadley 15"

Rev

X02

Date

Friday, June 21, 2013

Sheet


89

 of

101

(Blanking)

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Title

Reserved

Size
A3

Document Number
Hadley 15"


Date
Friday, June 21, 2013

Rev
X02

Sheet 90 of 101

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<Core Design>



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Title

Reserved

Size
A3

Document Number
Hadley 15"


Date
Friday, June 21, 2013

Rev
X02

Sheet 91 of 101

(Blanking)

<Core Design>



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Title

Reserved

Size

A3

Document Number

Hadley 15"

Date

Friday, June 21, 2013

Rev

X02

Sheet


92

 of

101

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Title

Reserved

Size

A3

Document Number

Hadley 15"

Date

Friday, June 21, 2013

Rev

X02

Sheet


93

 of

101

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Reserved

Size A3	Document Number Hadley 15"	Rev X02
Date Friday, June 21, 2013	Sheet 94	of 101

(Blanking)

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Title

Reserved

Size

Document Number

Rev

Hadley 15"

X02

Date

Friday, June 21, 2013

Sheet

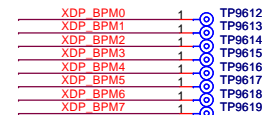
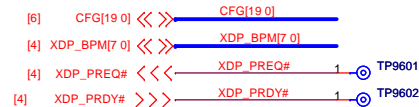
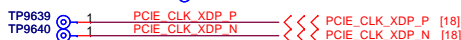
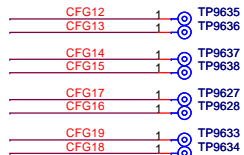
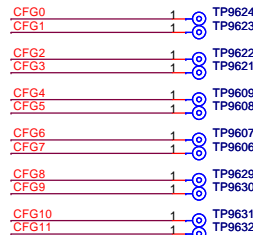
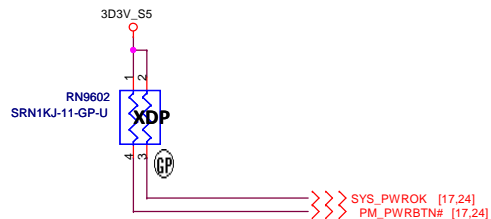
95

of

101

SSID = XDP

CPU XDP



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Title

CPU XDP

Size

Document Number

Hadley 15"

Rev

X02

Date

Friday, June 21, 2013

Sheet

96

of

101

PCH Strapping

Name	Schematics	Notes

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION

PCIE Routing

LANE1	X
LANE2	X
LANE3	Mini Card1(WLAN)
LANE4	X
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	
3	
4	
5	


USB Table

Pair	Device
0	USB port 1,with Power Share
1	USB 2.0 HDMI
2	USB port2 (usb redriver)
3	X
4	Touch Panel
5	Card Reader
6	BLUETOOTH
7	CAMERA

SMBus ADDRESSES

I ² C / SMBus Addresses	CHIEF RIVER ORB	
	Address	Bus
EC SMBus 1 Battery 0 CHARGER FS8122(HDMI Switch) (Bottom Dock) USB3.0 redriver PS8710 (Bottom Dock)	0x16 0x12 0x9E 0x40	BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 Battery 1 PCH Discrete VGA Thermal PS8321 HDMI level shifter NCT7718W	0x16 0x96 & 0x94 0x9C or 0x9E 0x96 & 0x97 0x98 or 0x99	SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
EC SMBus 3 NCT5605Y-0 NCT5605Y-1	0x30 0x32	SMB2_CLK/SMB2_DATA SMB2_CLK/SMB2_DATA SMB2_CLK/SMB2_DATA
PCH SMBus SO-DIMMA SO-DIMMB Intel LAN 82579 G-Sensor MINI WLAN INTEL LAN82579		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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Table of Content

Size A3Document NumberHadley 15"Rev X02

Date Friday, June 21, 2013Sheet 97 of 101

<Core Design>



Wistron Corporation
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Title

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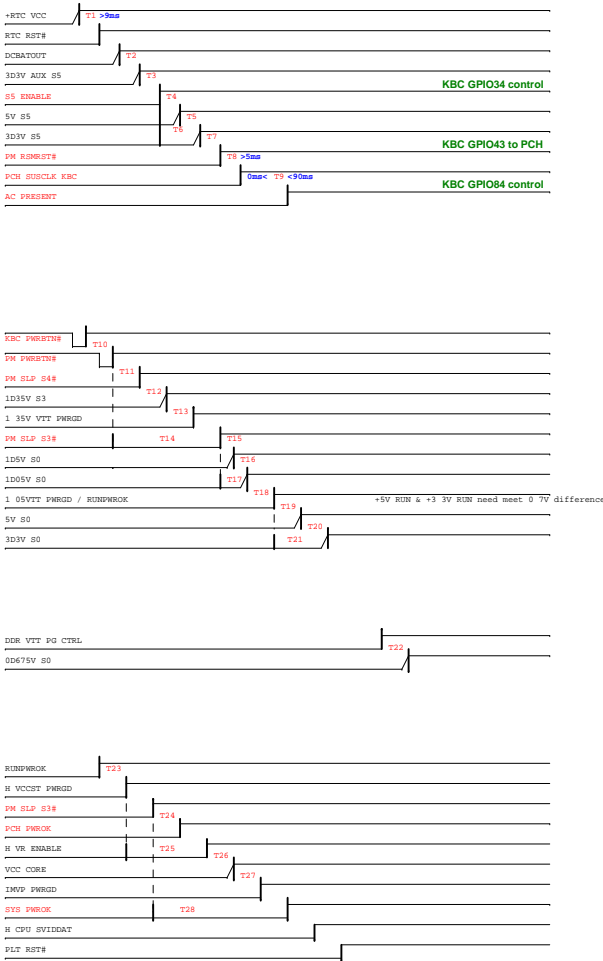
Size	Document Number	Rev
	Hadley 15"	X02

Date	Friday, June 21, 2013	Sheet	98	of	101
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Intel-Power Up Sequence

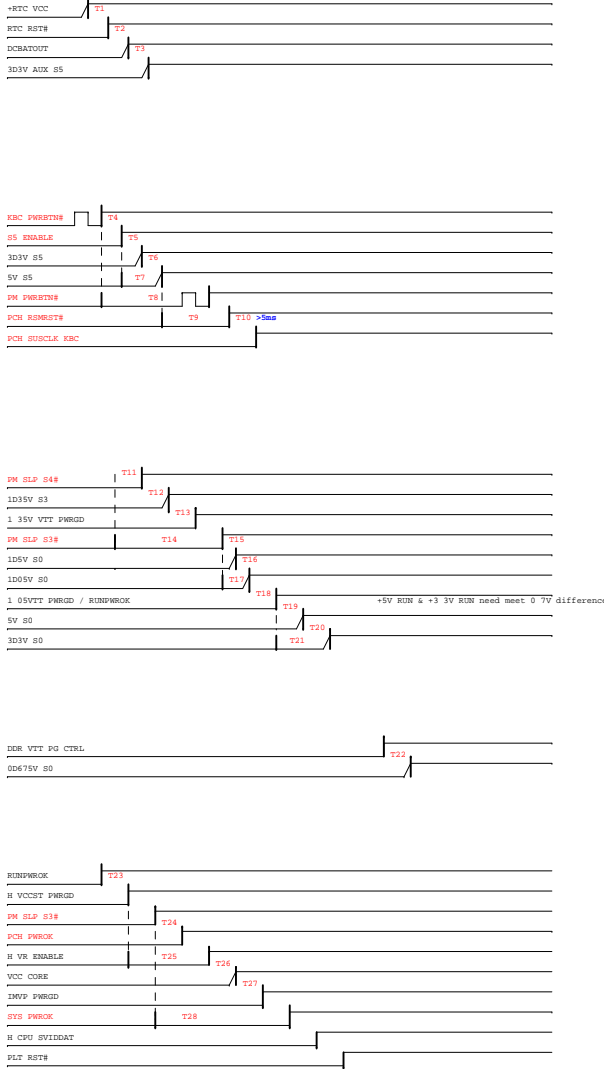
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Red printings:KBC GPIO involved

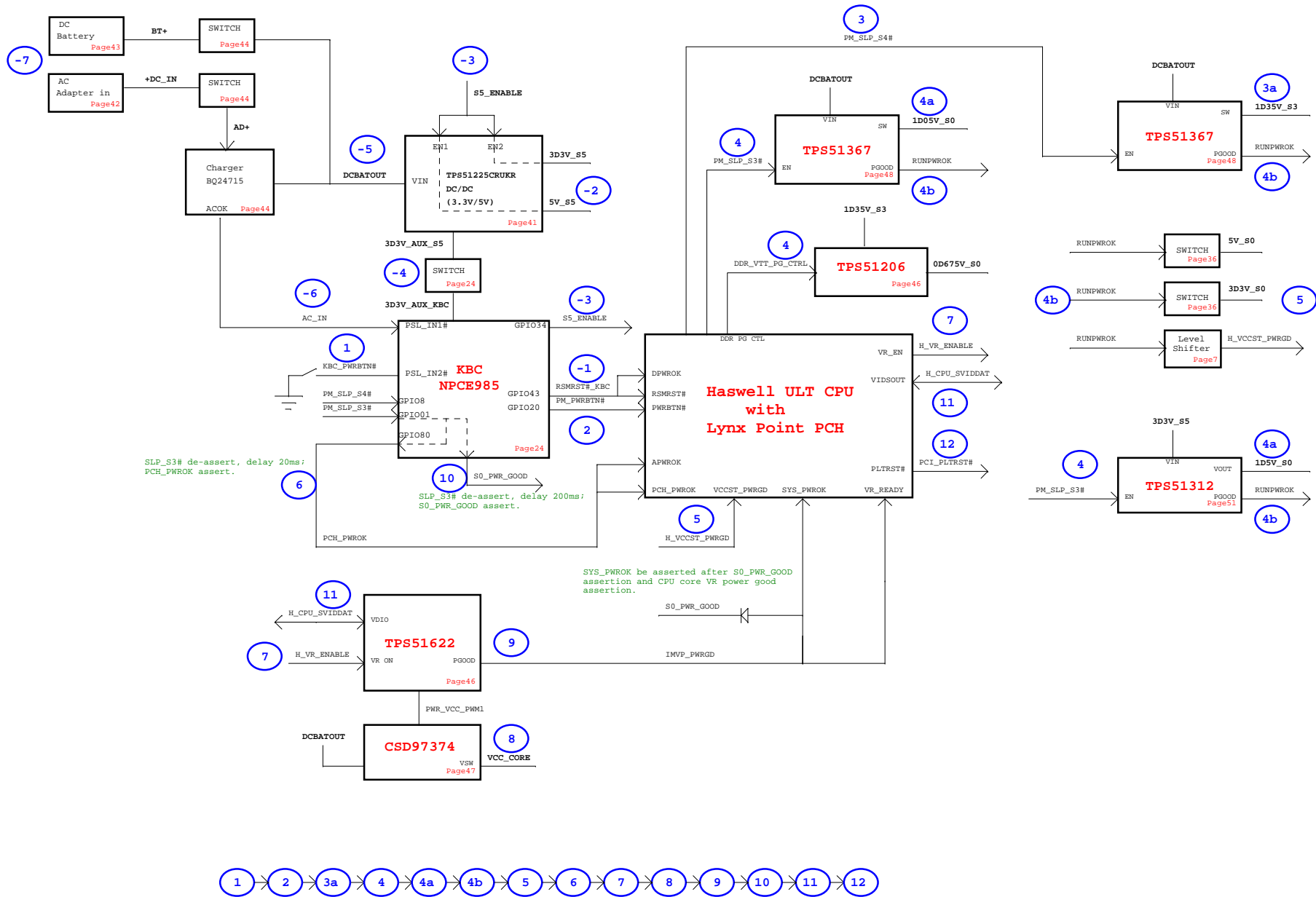


(DC mode)

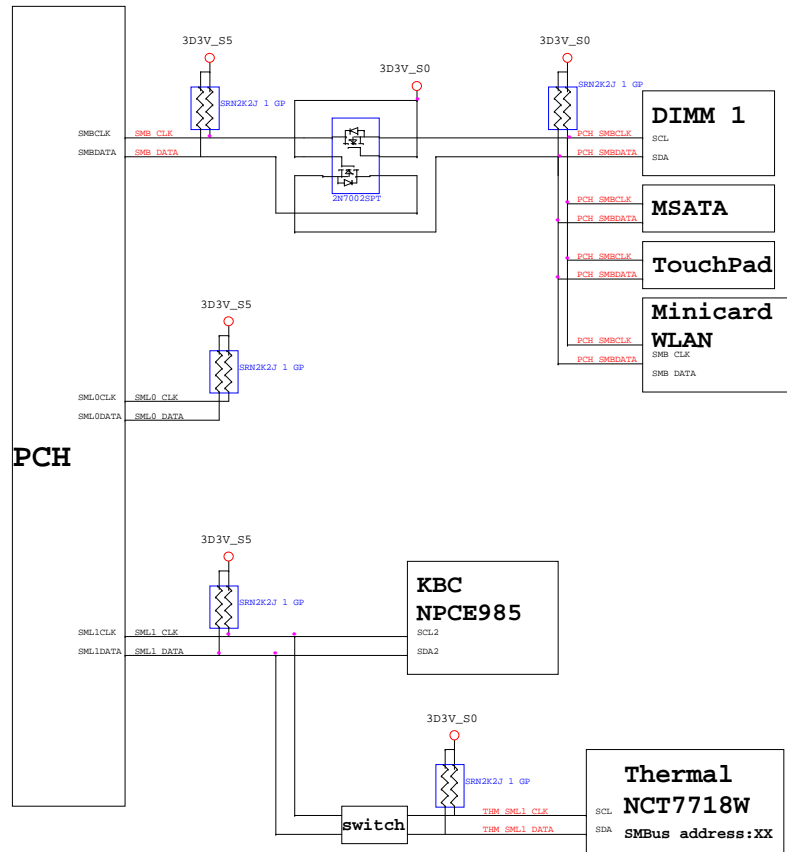
Red printings:KBC GPIO involved



Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



PCH SMBus Block Diagram



KBC SMBus Block Diagram

